

# AOD609

## Complementary Enhancement Mode Field Effect Transistor

### General Description

The AOD609 uses advanced trench technology MOSFETs to provide excellent  $R_{DS(ON)}$  and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications.

- RoHS Compliant
- Halogen Free\*

### Features

#### n-channel

$V_{DS}$  (V) = 40V,  $I_D$  = 12A ( $V_{GS}=10V$ )

$R_{DS(ON)} < 30m\Omega$  ( $V_{GS}=10V$ )

$R_{DS(ON)} < 40m\Omega$  ( $V_{GS}=4.5V$ )

#### p-channel

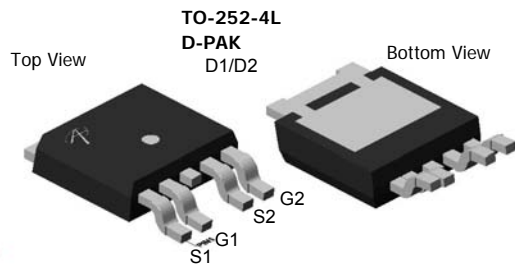
$V_{DS}$  (V) = -40V,  $I_D$  = -12A ( $V_{GS}=-10V$ )

$R_{DS(ON)} < 45m\Omega$  ( $V_{GS}=-10V$ )

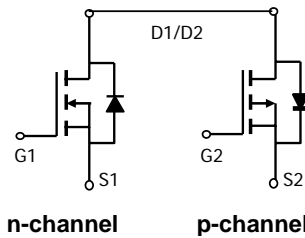
$R_{DS(ON)} < 66m\Omega$  ( $V_{GS}=-4.5V$ )

**100% UIS Tested!**

**100% Rg Tested!**



Top View  
Drain Connected to  
Tab



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	$V_{DS}$	40	-40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V
Continuous Drain Current <sup>B,H</sup>	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$	$I_D$	12	A
			-12	
Pulsed Drain Current <sup>B</sup>	$I_{DM}$	30	-30	
Avalanche Current <sup>C</sup>	$I_{AR}$	14	-20	
Repetitive avalanche energy $L=0.1\text{mH}^C$	$E_{AR}$	9.8	20	mJ
Power Dissipation	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$	$P_D$	27	W
			14	
Power Dissipation	$T_A=25^\circ\text{C}$ $T_A=70^\circ\text{C}$	$P_{DSM}$	2	W
			1.3	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	-55 to 175	$^\circ\text{C}$

### Thermal Characteristics: n-channel and p-channel

Parameter	Symbol	Device	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A,D</sup>	$R_{\theta JA}$	n-ch	17.4	25	$^\circ\text{C/W}$
$t \leq 10\text{s}$					
Maximum Junction-to-Ambient <sup>A,D</sup>	$R_{\theta JA}$	n-ch	50	60	$^\circ\text{C/W}$
Steady-State					
Maximum Junction-to-Lead <sup>C</sup>	$R_{\theta JC}$	n-ch	4	5.5	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A,D</sup>	$R_{\theta JA}$	p-ch	16.7	25	$^\circ\text{C/W}$
$t \leq 10\text{s}$					
Maximum Junction-to-Ambient <sup>A,D</sup>	$R_{\theta JA}$	p-ch	50	60	$^\circ\text{C/W}$
Steady-State					
Maximum Junction-to-Lead <sup>C</sup>	$R_{\theta JC}$	p-ch	3.5	5	$^\circ\text{C/W}$

**N Channel Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	40			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =250μA	1.7	2.5	3	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	30			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =12A T <sub>J</sub> =125°C		24 37	30 46	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =8A		31	40	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =12A		25		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.76	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				2	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =20V, f=1MHz		516	650	pF
C <sub>OSS</sub>	Output Capacitance			82		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			43		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		4.6	6.9	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, I <sub>D</sub> =12A		8.3	10.8	nC
Q <sub>gs</sub>	Gate Source Charge			2.3		nC
Q <sub>gd</sub>	Gate Drain Charge			1.6		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, R <sub>L</sub> =1.4Ω, R <sub>GEN</sub> =3Ω		6.4		ns
t <sub>r</sub>	Turn-On Rise Time			3.6		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			16.2		ns
t <sub>f</sub>	Turn-Off Fall Time			6.6		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =12A, di/dt=100A/μs		18	24	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =12A, di/dt=100A/μs		10		nC

A: The value of R<sub>θJA</sub> is measured with the device in a still air environment with T<sub>A</sub> =25°C. The power dissipation P<sub>DSM</sub> and current rating I<sub>DSM</sub> are based on T<sub>J(MAX)</sub>=150°C, using the steady state junction-to-ambient thermal resistance.

B: The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C.

D: The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175°C. The SOA curve provides a single pulse rating.

G: These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C.

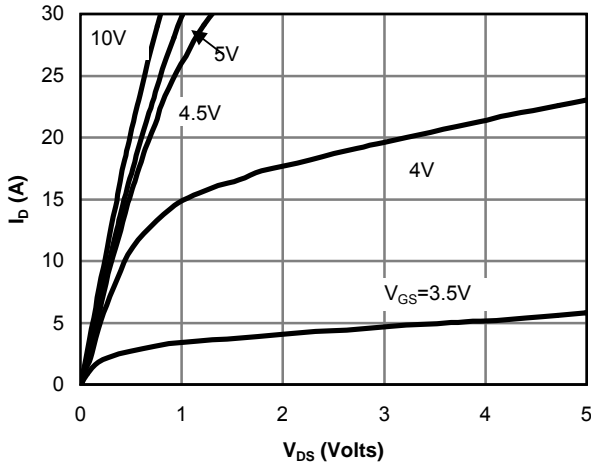
H: The maximum current rating is limited by bond-wires.

\*This device is guaranteed green after data code 8X11 (Sep 08 2008).

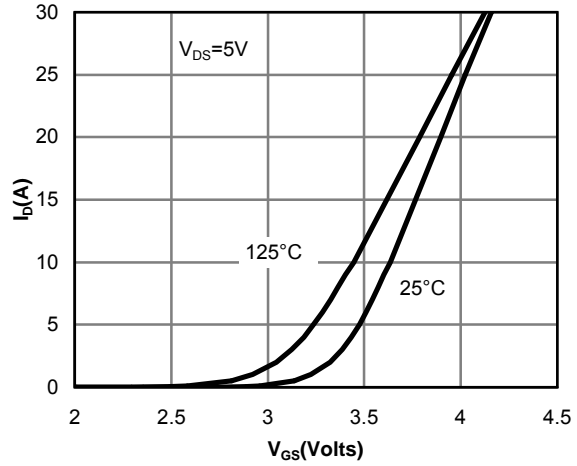
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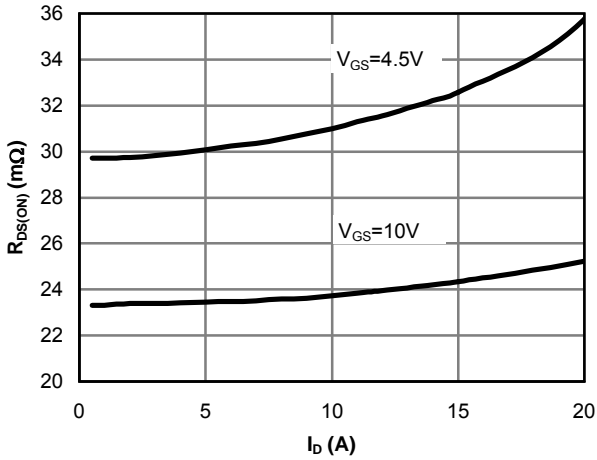
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: N-CHANNEL**



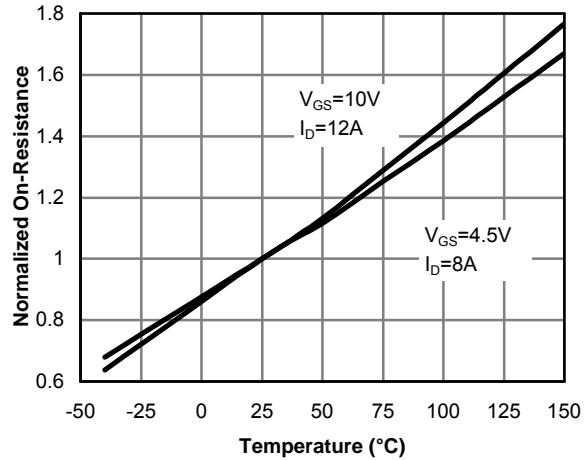
**Fig 1: On-Region Characteristics**



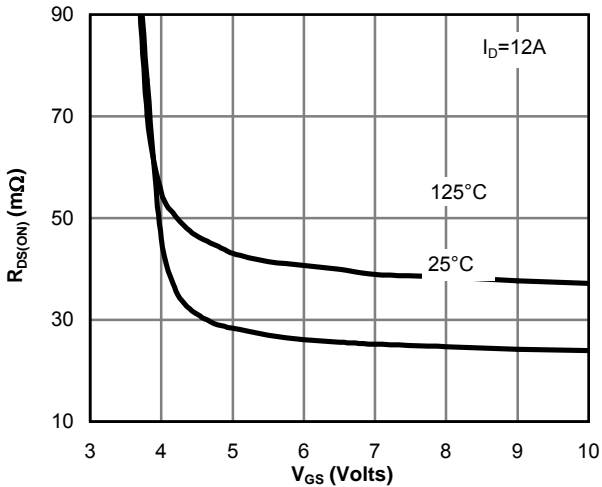
**Figure 2: Transfer Characteristics**



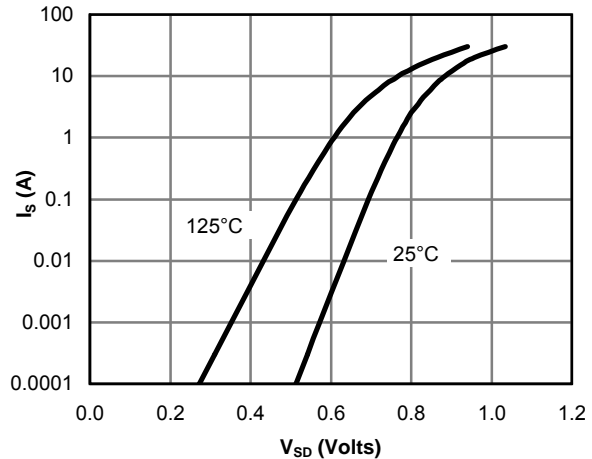
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**



**Figure 4: On-Resistance vs. Junction Temperature**



**Figure 5: On-Resistance vs. Gate-Source Voltage**



**Figure 6: Body-Diode Characteristics**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: N-CHANNEL**

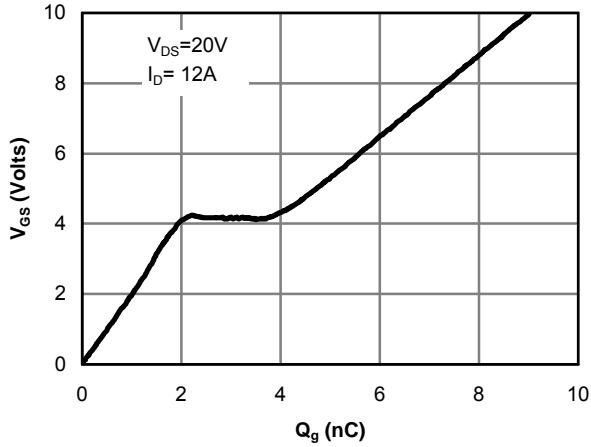


Figure 7: Gate-Charge Characteristics

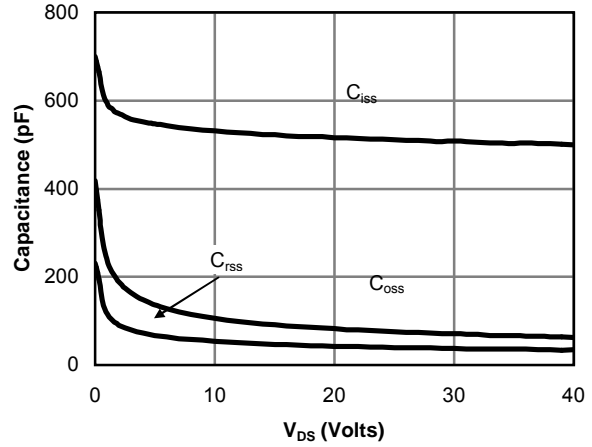


Figure 8: Capacitance Characteristics

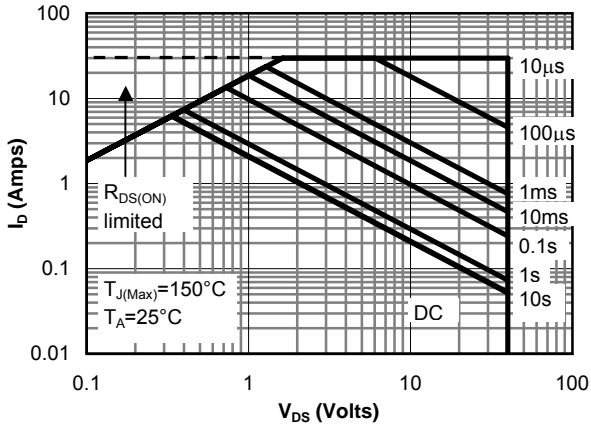


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

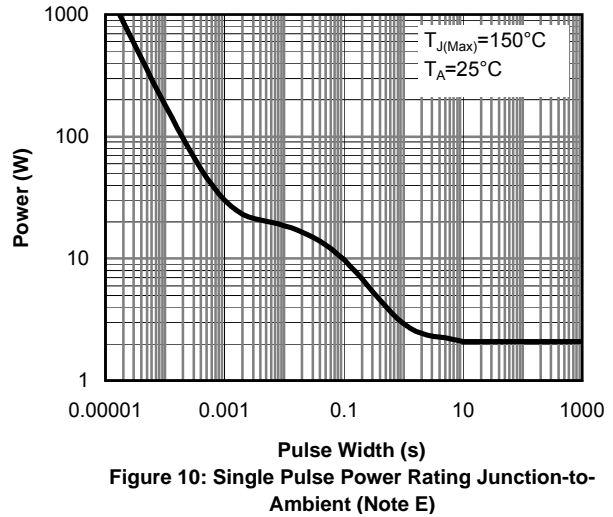


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

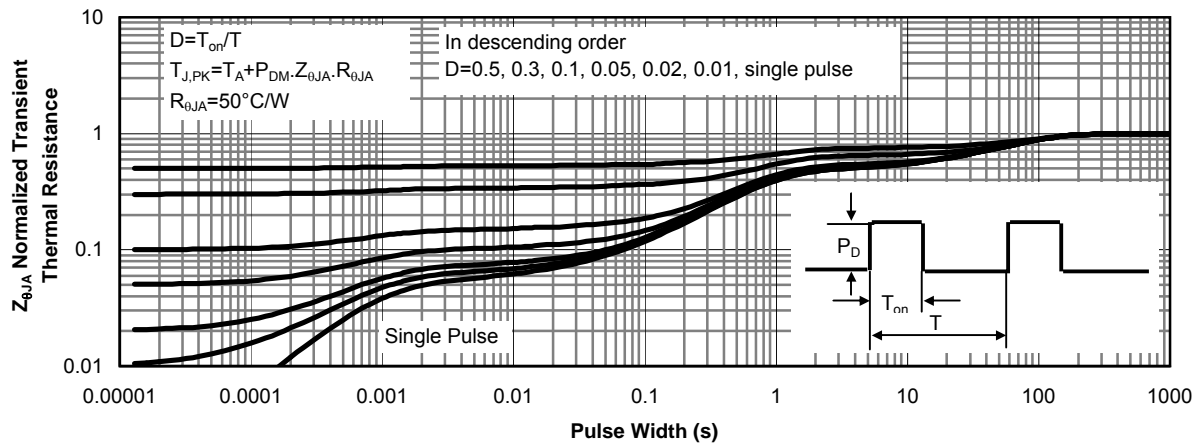
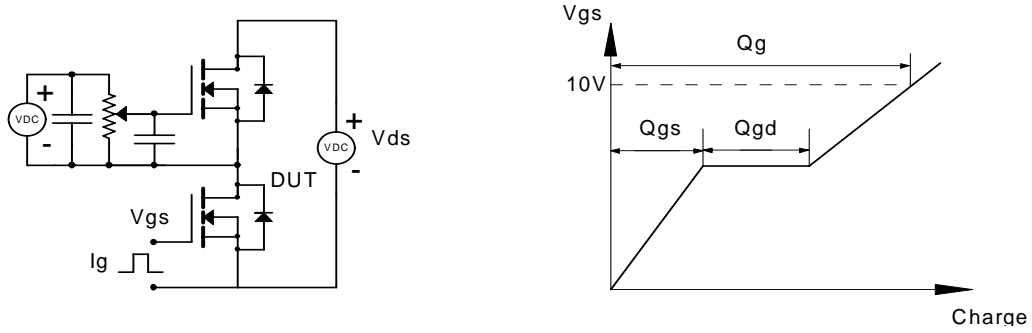
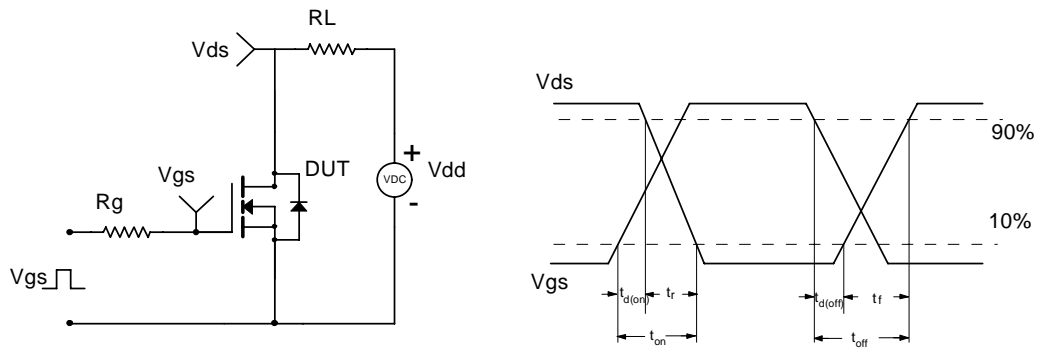


Figure 11: Normalized Maximum Transient Thermal Impedance

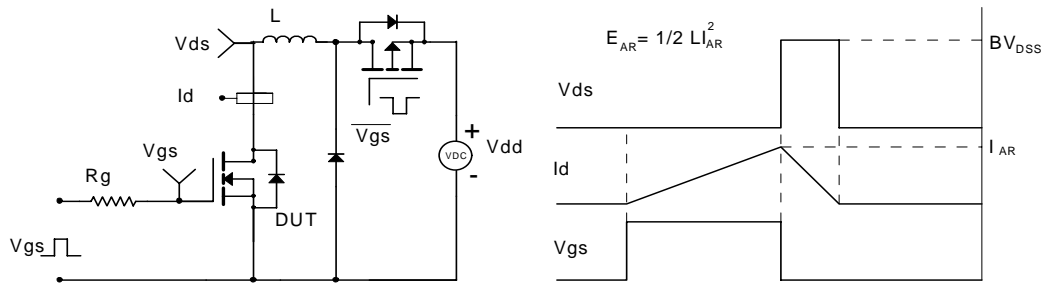
Gate Charge Test Circuit & Waveform



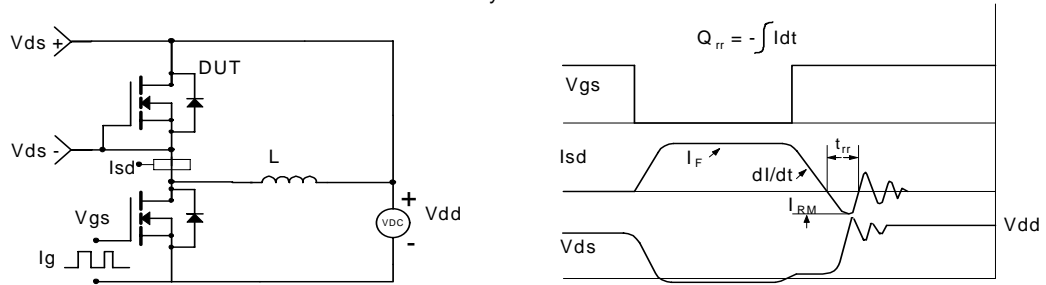
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



**P-Channel Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> = -250μA, V <sub>GS</sub> =0V	-40			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -40V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-1 -5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> = -250μA	-1.7	-2	-3	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> = -10V, V <sub>DS</sub> = -5V	-30			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = -10V, I <sub>D</sub> = -12A T <sub>J</sub> =125°C		36 52	45 65	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -8A		51	66	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = -5V, I <sub>D</sub> = -12A		22		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> = -1A, V <sub>GS</sub> =0V		-0.76	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				-2	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance			900	1125	pF
C <sub>oss</sub>	Output Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> = -20V, f=1MHz		97		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			68		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		14		Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (-10V)	Total Gate Charge			16.2	21	nC
Q <sub>g</sub> (-4.5V)	Total Gate Charge	V <sub>GS</sub> = -10V, V <sub>DS</sub> = -20V, I <sub>D</sub> = -12A		7.2	9.4	nC
Q <sub>gs</sub>	Gate Source Charge			3.8		nC
Q <sub>gd</sub>	Gate Drain Charge			3.5		nC
t <sub>D(on)</sub>	Turn-On Delay Time			6.2		ns
t <sub>r</sub>	Turn-On Rise Time	V <sub>GS</sub> = -10V, V <sub>DS</sub> = -20V, R <sub>L</sub> =1.4Ω, R <sub>GEN</sub> =3Ω		8.4		ns
t <sub>D(off)</sub>	Turn-Off Delay Time			44.8		ns
t <sub>f</sub>	Turn-Off Fall Time			41.2		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> = -12A, dI/dt=100A/μs		21	27	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> = -12A, dI/dt=100A/μs		14		nC

A: The value of R<sub>θJA</sub> is measured with the device in a still air environment with T<sub>A</sub>=25°C. The power dissipation P<sub>DSM</sub> and current rating I<sub>DSM</sub> are based on T<sub>J(MAX)</sub>=150°C, using t ≤ 10s junction-to-ambient thermal resistance.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175°C. The SOA curve provides a single pulse rating.

G. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C.

H. The maximum current rating is limited by bond-wires.

\*This device is guaranteed green after data code 8X11 (Sep 9<sup>th</sup> 2008).

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL

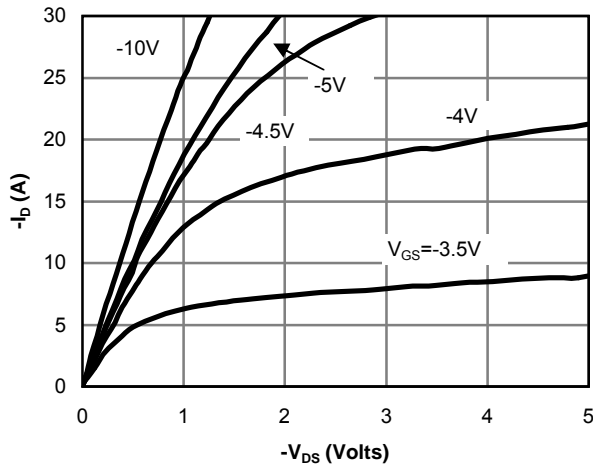


Fig 12: On-Region Characteristics

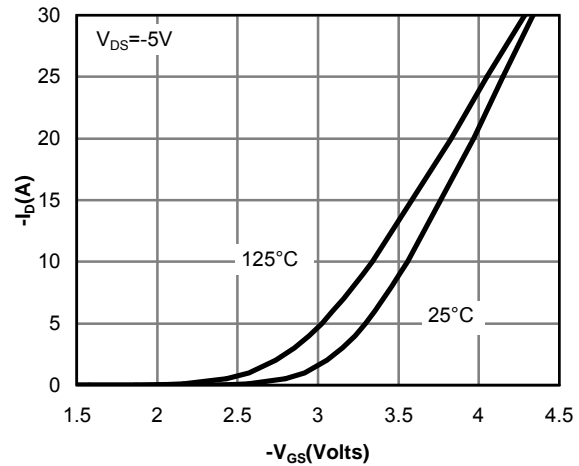


Figure 13: Transfer Characteristics

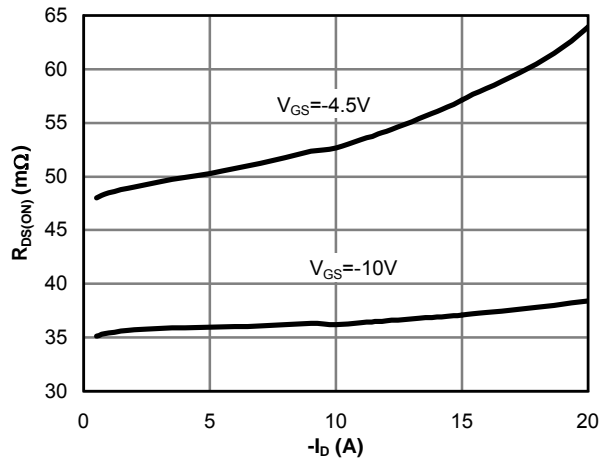


Figure 14: On-Resistance vs. Drain Current and Gate Voltage

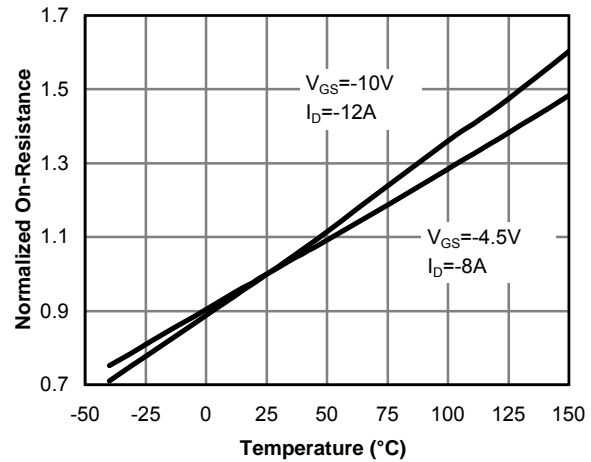


Figure 15: On-Resistance vs. Junction Temperature

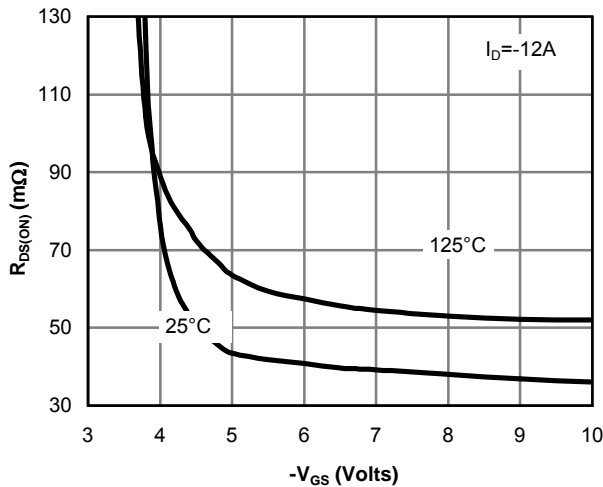


Figure 16: On-Resistance vs. Gate-Source Voltage

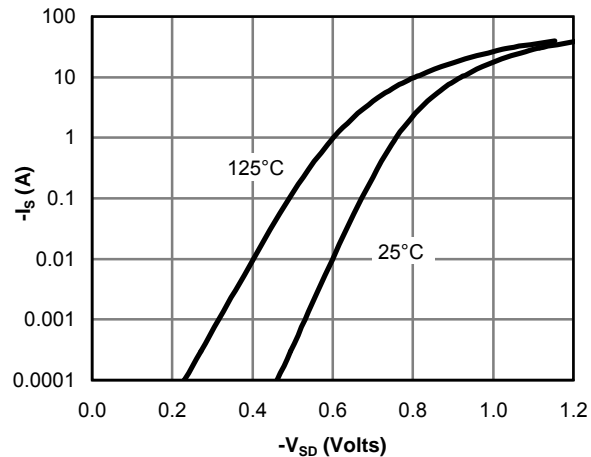


Figure 17: Body-Diode Characteristics

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL**

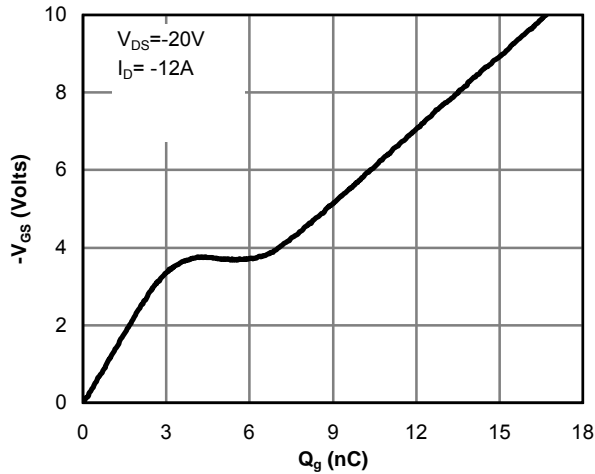


Figure 18: Gate-Charge Characteristics

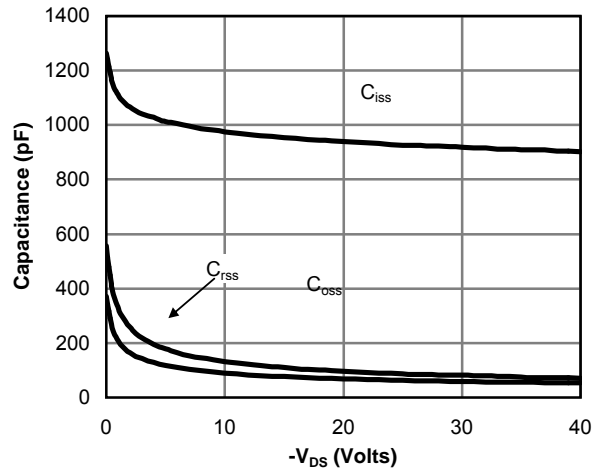


Figure 19: Capacitance Characteristics

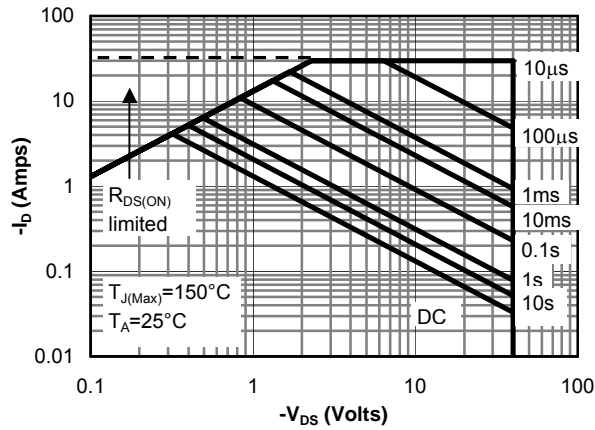


Figure 20: Maximum Forward Biased Safe Operating Area (Note E)

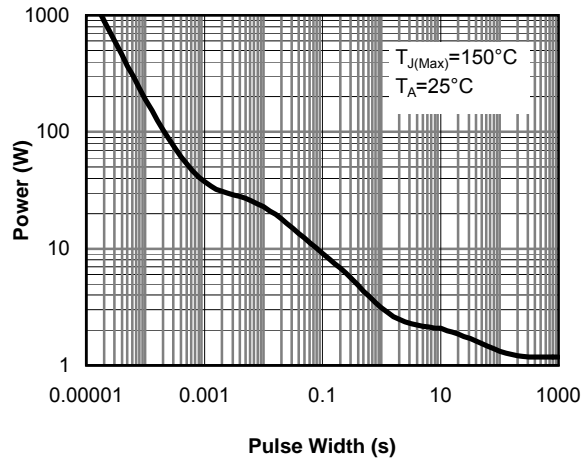


Figure 21: Single Pulse Power Rating Junction-to-Ambient (Note E)

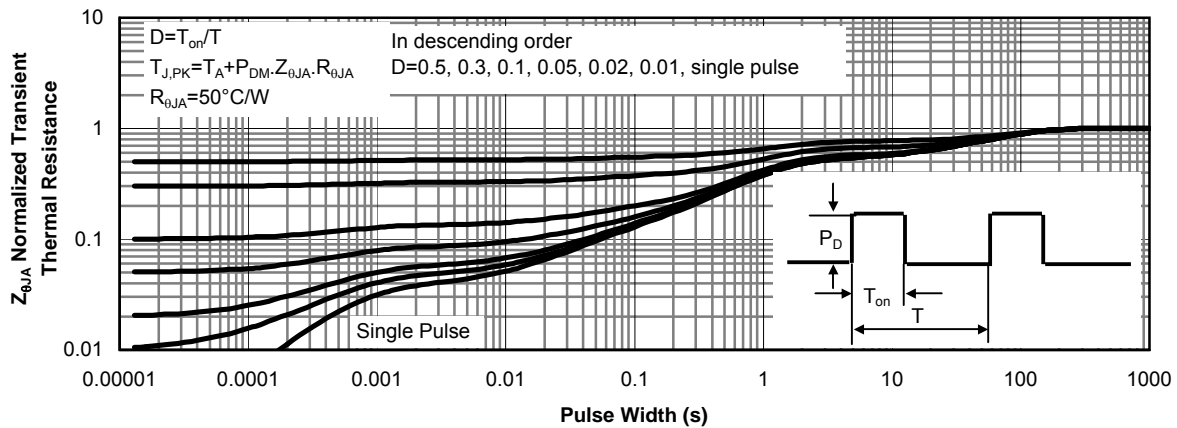
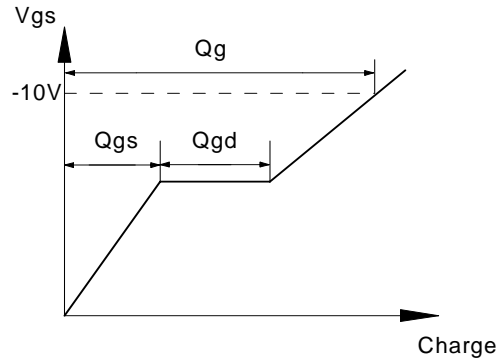
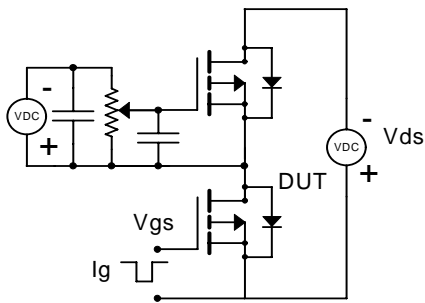


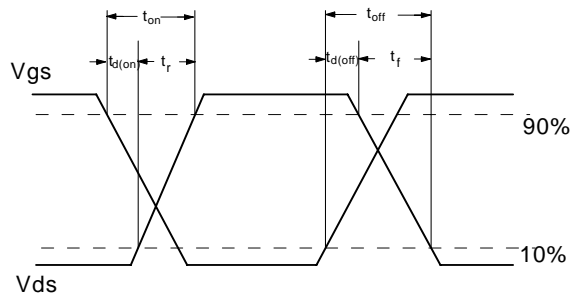
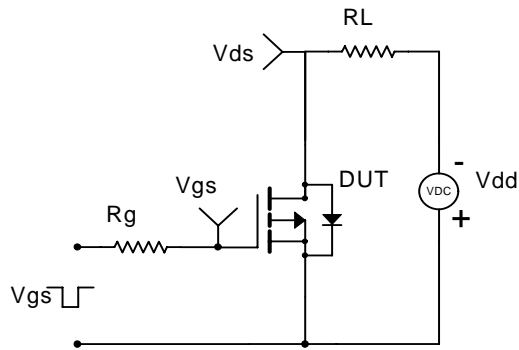
Figure 22: Normalized Maximum Transient Thermal Impedance



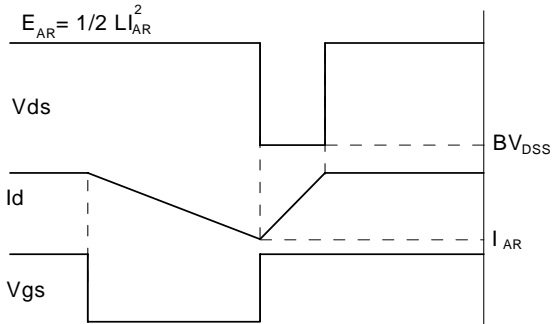
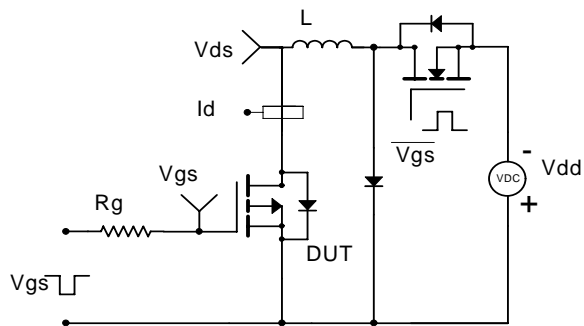
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

