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Ultra High Performance Broadband 12 to 16-Bit Data Acquisition Platform

ISLA214P50-55210EV1Z High Speed ADC/AMP Evaluation Board

1. ISLA214P50 High Speed, High Performance ADC (14-bit, 500MSPS)
2. ISL55210 High Performance, Low Power, Fully Differential Amplifier (FDA)
3. Compatible with existing Intersil high speed ADC evaluation platforms
4. Optional response measurement port from ADC inputs to board edge
5. Pin compatible family of 12-to-16 bit ADC's can be used on this board

Performance Range

1. Clock rate range: 80MSPS to 500MSPS
2. 283mV$_{P-P}$ input (-7.0dBm) for -2dBFS at ADC inputs (1.6V$_{P-P}$ at ADC)
3. ±0.8dB flat response from 100kHz to 100MHz
4. Typical SNRFS (30MHz input, 500MSPS): 71.8dBFS (vs 72.6dBFS for ADC only)
5. Typical SFDR (30MHz input, 500MSPS): 89dBc (vs 84dBc for ADC only)

System Requirements

1. ISLA214P50-55210EV1Z Evaluation Board
2. KMB-001LEVALZ Intersil Motherboard (+5V supply provided with motherboard)
3. Intersil Konverter software http://www.intersil.com/content/intersil/en/products/data-converters/high-speed-a-d-converters/hs-adc-evaluation-platform.html
4. Low jitter clock source
5. Bandpass filters
6. PC running Windows XP operating system with Konverter software installed

Board Numbering Note

The original board marking was ISLA214P50/55210EV1Z. For ordering purposes, that has been changed wherever possible to ISLA214P50-ISL55210EV1Z. Any reference to ISL214P50/55210EV1Z would be the same end item as the final ordering number version with the dash instead slash.

Evaluation Platform Overview

This ISLA214P50-55210EV1Z is an evaluation platform featuring Intersil's ultra-high dynamic range fully differential amplifier (FDA), the ISL55210, and the High Speed, High Performance, 14-bit, 500MSPS ADC, the ISLA214P50. This PCB daughterboard mates to Intersil's existing high speed ADC evaluation platform allowing for easy performance measurement and analysis (see Intersil Application Notes AN1433, and AN1434 for more information). The ADC evaluation platform consists of custom designed hardware and software supporting a wide range of ADC daughterboards on the KMB-001 motherboard. The function of the hardware is to provide power to the ADC daughterboard, manage the communication to the ADC internal settings, accept clock and signal inputs, and buffer the digital outputs for communication to a host PC. The Konverter software is required to configure the ADC for initial operation, to modify the device functionality or parameters, and to process and display the captured digital data. Konverter software version 1.22c (or later) supports the ISLA214P50 family and the ISLA214P50-55210EV1Z PCB.

CONTACT THE FACTORY FOR ASSISTANCE IN USING THE KONVERTER SOFTWARE TO MODIFY THIS BOARD TO A DIFFERENT ADC IN THE PIN COMPATIBLE FAMILY.

TABLE 1. PIN COMPATIBLE HIGH PERFORMANCE ADC FAMILY

PART NUMBER	RESOLUTION (Bits)	MAXIMUM SAMPLE RATE (Msps)	POWER CONSUMPTION (mW)
ISLA216P25	16	250	785
ISLA216P20	16	200	720
ISLA216P13	16	130	615
ISLA214P50	14	500	835/900 (Note)
ISLA214P25	14	250	450
ISLA214P20	14	200	410
ISLA214P13	14	130	360
ISLA214P12	14	125	310
ISLA212P50	12	500	823/892 (Note)
ISLA212P25	12	250	440
ISLA212P20	12	200	405
ISLA212P13	12	130	355

NOTE: I2E disabled/enabled.

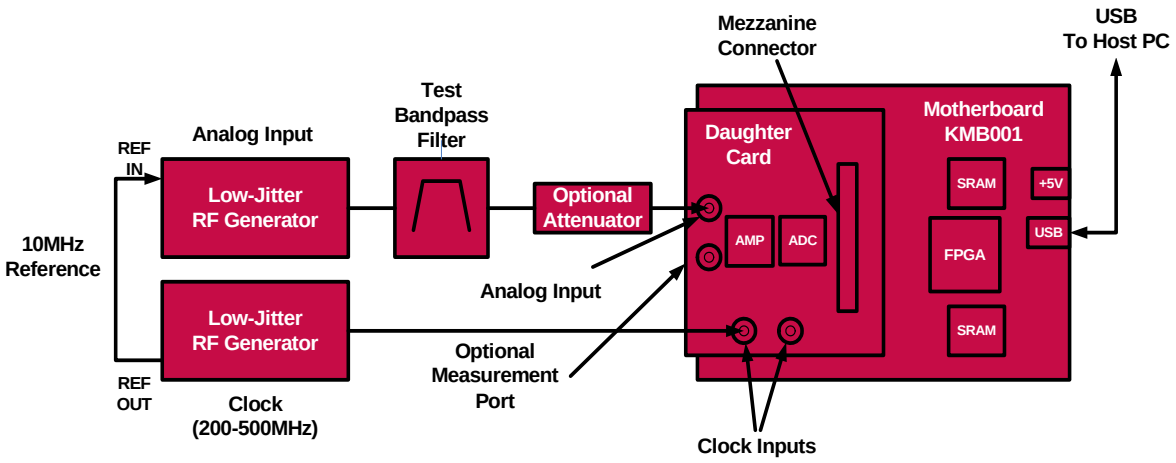

FIGURE 1. TYPICAL CHARACTERIZATION SETUP USING THE INTERSIL KMB-001 MOTHERBOARD AND KONVERTER SOFTWARE

OPERATING PRECAUTIONS:!!

IT IS STRONGLY RECOMMENDED TO INSERT THE +5V PLUG AT THE MOTHERBOARD PRIOR TO PLUGGING IN THE AC ADAPTER TO REDUCE THE POSSIBILITY OF POWER SURGES WHICH CAN DAMAGE THE PCB. PROBING ON THE PCB SHOULD BE DONE WITH CARE USING PROPER ESD TECHNIQUES WHILE HANDLING.

Hardware Description

There are two components in the hardware portion of the evaluation platform. The daughtercard and the motherboard (Figure 1). The FDA and ADC are on the daughtercard, which accepts power from the motherboard and contains the analog input circuitry, clock interface, and supply decoupling. The daughtercard interfaces to the motherboard through a mezzanine connector. The motherboard contains a USB interface, an FPGA and SRAM. The motherboard serves as the interface between the host PC and the ADC daughtercard. Most of the ADC functionality is controlled through the motherboard by the Konverter software. The FPGA accepts output data from the ADC and buffers it to the SRAMs before passing it to the PC at the lower data rate required for post-processing. The maximum buffer depth is approximately one million words.

The designer must supply a low jitter RF generator for the clock input to achieve the SNR reported here. Some possible options are shown in “Appendix A: Low Phase Noise RF Generators” on page 15. An alternate to a signal generator for fixed 500MSPS clock rates would be the 3.3V supply, SMA barrel, RFPRO33-500 from Crystek. A slight degradation in SNR might be expected using this device vs the best low phase noise RF signal generators and a bandpass filter on the clock. Using a bandpass filter on the clock will reduce clock jitter and improve SNR while using a bandpass on the signal source is normally required to eliminate harmonics while testing the board performance. Most RF generators that might be used as a test analog input source have very poor harmonic distortion and require a bandpass postfilter to see the full performance of the ADC’s FFT.

Software Description

The software component is the Konverter Analyzer, a graphical user interface (GUI) created with MATLAB™. A MATLAB Component Runtime engine is supplied, which executes a compiled version of the m-files. Therefore, a separate version of MATLAB is not required to run the Konverter Analyzer.

The GUI controls the ADC configuration through its SPI port, reads data from the motherboard and performs the post-processing and display of digitized data. Data can be viewed in either the time or frequency domain, and can be saved for later processing. Critical performance parameters such as SNR, SFDR, ENOB, etc. are calculated and displayed on the screen when FFT output is selected and a dominant single frequency is being applied.

Initial Start-Up

Referring to Figure 3, connect the daughtercard to the motherboard by aligning the two matching mezzanine connectors. Four screws on the motherboard align with the mounting holes on the daughtercard. Next, connect the clock source (≈12dBm level into 50Ω) which will be required for communication to the Konverter software. Then connect a test source or signal of interest coming from your signal channel at a maximum input level <350mV$_{P-P}$ (or <-5.1dBm for single tone). With the RF signal generators delivering a clock and input signal to the daughtercard, and the +5V supply jack plugged into the motherboard, plug the AC power plug into a wall socket. The daughtercard is powered from linear regulators on the motherboard through the mezzanine connector. The USB cable should now be connected from the motherboard to the PC. Be sure to use the same USB port that was originally used when the Konverter software was installed on the PC to insure it is recognized. Now launch the Konverter software on the PC where it should recognize the motherboard and proceed to taking an FFT.

Motherboard

The only connections to the motherboard are the +5V supply power and the USB cable to the PC with the Konverter software loaded. No additional configuration of the motherboard is required. IT IS STRONGLY RECOMMENDED TO INSERT THE +5V PLUG AT THE MOTHERBOARD WITH THE DAUGHTERBOARD ATTACHED PRIOR TO PLUGGING IN THE AC ADAPTER TO REDUCE THE POSSIBILITY OF POWER SURGES WHICH CAN DAMAGE THE PCB. PROBING ON THE PCB’S SHOULD BE DONE WITH CARE AND PROPER ESD PROCEDURES USED WHEN HANDLING THE BOARDS.

Software Start-Up

The FPGA clock is derived from the ADC output clock, and the FPGA clock must be active for the software to operate correctly. Therefore, it is critical to have a convert clock present and the board powered up before the Konverter software is launched. It is not necessary to have an analog input signal present.

The compressed MATLAB files are unpacked the first time the GUI is invoked after installation. This will slow the start-up the first time the evaluation system is used but it will run more quickly in subsequent startups. Complete information can be found in the KMB-001 Installer manual at: http://www.intersil.com/converters/adc_eval_platform/

The main Konverter Analyzer window is shown in Figure 16. The application opens in FFT mode by default, but other modes can be selected using the radio buttons in the lower left corner. In each mode, relevant parameters are displayed in the data box the left side of the window.

The following data is displayed in all operating modes –

1. Fsamp: Sample clock frequency, automatically detected.
2. Ffund: Input frequency, automatically detected if input is a single tone or dominant tone waveform
3. Fund: Amplitude of the dominant tone in dBFS
4. Samples: Record length, defaults but can be updated

Data Acquisition

Normally, the first step to an FFT data display is to open the “Setup” key in the upper left and pick a windowing function to limit spectral leakage. All the plots and data here used the Blackman Harris 4 term windowing. It is also possible to change the record length for the FFT in this screen. Normally, the continuous calibration and background keys are selected and, if desired, an averaging of the FFT outputs may be selected in the lower left of the Konverter screen set up for FFT display (default at start-up). Then, press “Run” in the lower left and the FFT will be updating. The number of averaged sweeps defaults to 10, but can also be changed in the “Setup” conditions dialog window.

Menu items and the toolbar buttons may not function properly if data is being captured continuously. Press “Stop” in the lower left before selecting a menu item or using a toolbar button.

AN1433 should be consulted for more information on the options provided in the Konverter windows. AN1434 offers help for first time installation if needed.

Hardware and Analog Signal Path Description

Figure 2 shows a close-up of the ISLA214P50-55210EV1Z daughtercard.

The SMA at the top left is the analog input connection, the next one down is an optional sense port for an attenuated version of the differential signal being presented to the ADC input pins, while the lower SMA is the clock input pin. Several optional inputs are not populated, like the amplifier disable control line at the lower left of the card and some alternate clock input paths on the bottom. The V_{TEST} path SMA is not populated on the board as delivered but may be easily added.

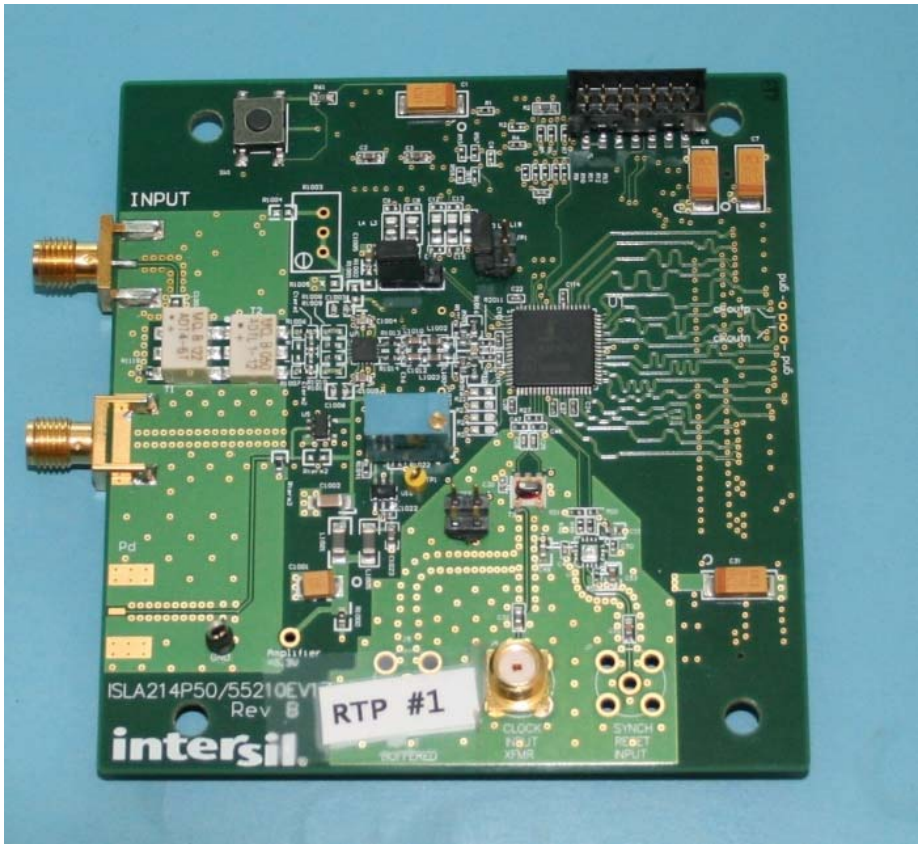

FIGURE 2. ISLA214P50-55210EV1Z DAUGHTERBOARD

FIGURE 3. ISLA214P50-55210EV1Z DAUGHTERBOARD ON KMB-001 MOTHERBOARD

The analog input signal comes in through 2-MiniCircuits transformers then into the ISL55210 then into an interstage passive RLC filter to the ADC. The blue potentiometer in the middle of the board is a common mode voltage adjustment for the average DC voltage applied to the ADC inputs for this AC coupled signal path. This board plugs into the KMB-001 motherboard to appear as in Figure 3.

Here, the input signal is connected and the 500MHz clock is being applied through a TTE 500MHz Bandpass filter. The power is being applied to the motherboard as shown by the active green light just under the +5V power connector in the upper right. Again, the +5V board connector is plugged in first, then the AC plug inserted to the power allowing the power brick to filter the +5V power up transient. Similarly on power down, unplug the +5V power at the AC plug side.

While the full signal path schematic is shown in Figure 46, it is best to break it into pieces for discussion of design, performance, and options. In general, the board offers numerous optional connections that are indicated in green on the schematic and/or by DNP for the standard board build. The basic signal path is intended to:

1. Terminate a single ended input with an AC-coupled, broadband, 50Ω impedance. This is of course expecting the source to also be a broadband 50Ω source and that impedance does get reflected through the input transformers to be part of the signal chain flatness characteristic.
2. Convert the single ended input to the required differential signal at the ADC inputs centered within the converter's desired common mode voltage range.
3. Provide amplification from a nominal -7dBm ($283mV_{P-P}$) single tone input to a -2dBFS (2dB below the $2V_{P-P}$ full scale of the ADC) or $1.58V_{P-P}$ at the ADC input pins with extremely low noise and distortion. This 5.6V/V gain (15dB) gain is a combination of the input transformer step up, ISL55210 gain, and various insertion losses in the transformers and interstage filter from the ISL55210 to the ADC.
4. As part of the interstage filter design, this board includes a V_{CM} control loop that senses the average DC voltage at the two ADC inputs and servo's a control voltage into the filter design to match a reference voltage applied to the servo loop op amp. The board is delivered set to 0.96V as that has shown improved SFDR for the filter source impedance and the ISLA214P50 ADC. Changing ADC selections and/or filter designs in this board might benefit from a different nominal V_{CM} control target for best SFDR and the V_{CM} adjust pot allows and easy means to test that.

AMPLIFIER POWER SUPPLY DECOUPLING ISSUES

The portion of the signal path schematic of Figure 4 shows one example of good power supply decoupling for this single 3.3V supply amplifier. Where possible, a large valued capacitor isolated towards this 4GHz amplifier with a high frequency ferrite and then another 1µF element provides a PI filter on the board. Right at the 2 device supply pins, X2Y capacitors are used to get the best high frequency decoupling. These 0.1µF elements actually are two capacitors connected in parallel to give 0.2µF decoupling with much lower ESR and higher self resonant frequency than typical ceramic SMD capacitors. Standard SMD 0.1µF ceramic capacitors can be used instead but may increase the even order harmonics at higher frequencies as they go self resonant. Those are provisioned on the board as optional elements but not populated as shown in Figure 4 by the green capacitors C1003 and C1008.

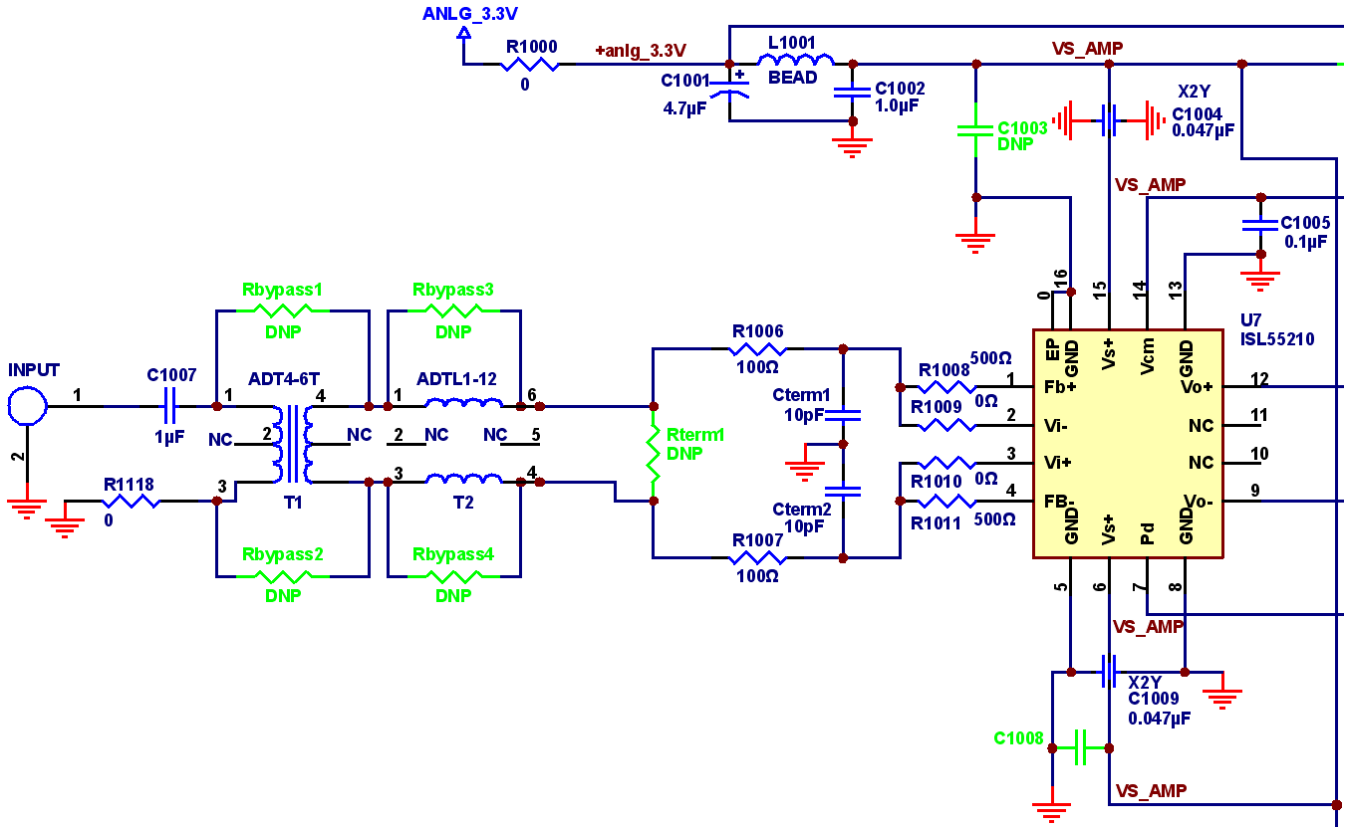

FIGURE 4. AMPLIFIER POWER SUPPLY DECOUPLING AND INPUT SIGNAL UP TO THE AMPLIFIER INPUTS

INPUT SIDE CIRCUIT DESIGN AND OPTIONS

As delivered, the interface uses an input transformer that is very flat to low frequencies followed by a common mode choke transformer that is a DC short for biasing with <0.3dB insertion loss to >1GHz for the differential signal. Either may be removed and replaced by shorts or resistor elements using the bypass resistors.

The input signal is coupled through a 1µF blocking cap (to protect against accidental DC shorts) to an input step up transformer and then directly into a common mode choke transformer. The 1:2 turns (1:4Ω) ratio step up transformer offers many advantages combined with an FDA as shown here. The second transformer provides a differential signal short but a common mode open circuit. Differentially, the two 100Ω gain resistors appear directly at the output of the input step up transformer.

Briefly, the 2-100Ω series resistors feed into a differential virtual ground at the FDA summing junctions (R1009&R1010 in Figure 4) and form a 200Ω differential termination impedance for the ADT4-6T. That is input referred as a broadband 50Ω termination impedance out of the 1µF blocking cap. Scaling these resistors up, while still maintaining a 200Ω secondary termination, can be done using the Rterm1 element. This is sometimes useful at lower gain targets to allow the feedback resistors (R1008 & R1011) to be scaled up when they might be adding significant loading to the output stage of the ISL55210. Detailed specifications for 4GHz gain bandwidth product, 0.85nV/√Hz input noise ISL55210 may be found at: http://www.intersil.com/products/ISL55210

The ISL55210 provides duplicates of the differential outputs on the input side for tighter signal path layout. The feedback resistors are the 2 -500Ω elements where the connection back into the inverting summing junctions are the 0Ω elements. Neglecting transformer insertion losses, the gain from the input port to the amplifier outputs should be 2 (in the first transformer) X 5 (in the FDA) = 10 (or 20dB). The ADT4-6T was selected primarily for its excellent flatness and distortion down to 100kHz. Its measured response showed a -1dB flatness span from 40kHz to 178MHz when driven from 50Ω to 200Ω load with a -0.18dB midband insertion loss. This is a suitable frequency span for the intended 100kHz to 100MHz digitizer bandwidth in this board. It does show a bit of rolloff at 100MHz which is partially equalized by the 10pF capacitors to ground at the summing junctions in Figure 4. Adding those capacitors does start to peak the output noise of the ISL55210, but this stage will be followed by a passive filter rolling that noise off. A detailed discussion of the input referred noise figure for this transformer coupled FDA topology may be found at: http://www.edn.com/design/analog/4400484/Accurately-predict-measured-noise-figures-for-transformer-coupled-differential-amplifiers--Part-1-of-2--

For the default configuration on this ISLA214P50-55210EV1Z board using the components shown in Figure 4, the estimated noise figure will be 7.2dB from a 50Ω source. Converting that to an input referred spot noise voltage including a 50Ω source noise gives a very low 1.02nV/√Hz. This is only for the amplifier stage, and not including any noise in the original source signal. Delivering this to the ADC inputs through the full signal path gain

of 5.6V/V yields a 5.7nV/√Hz differential spot noise. Combining this with the various noise elements within the ISLA214P50 will give a slight degradation in the resulting SNR in the FFT. Those calculations are described in this article: “Deliver the lowest distortion and noise in a low power, wideband, ADC interface – Part 2 of 4”
http://www.planetanalog.com/document.asp?doc_id=528177

The second ADTL1-12 common mode choke transformer provides a very broadband, low insertion loss, element that forces balance in this differential signal path. Testing with and without this element showed a significant improvement in the FDA output 2nd harmonic distortion at higher frequencies. This is an optional element in the design and can be bypassed with the optional shorts, but the best SFDR will be achieved with this element included as it is in the standard board build.

ELEMENTS CONTRIBUTING TO THE PASSBAND FLATNESS AND HIGHER FREQUENCY CUTOFF

Each of the elements in the signal path have fine scale rolloffs that need to be considered to achieve the final ±0.8dB flatness through the 100kHz to 100MHz intended digitizer range for this example design board.

The ADT4-6T input transformer was selected mainly for its low frequency performance. While specified as -1dB flat from 150kHz to 200MHz, typical devices measure to have a -1dB flatness span when driven from a 50Ω source to a 200Ω load of 40kHz to 180MHz. This far exceeds the Mini-Circuits specified flatness region on the low frequency side which is very typical for these wideband baluns.

Figure 5 shows a comparison to measured and modeled transformer response with a 50Ω source to 200Ω load. Since there is limited data at low frequencies in the vendor data sheet, no comparison is made to that.

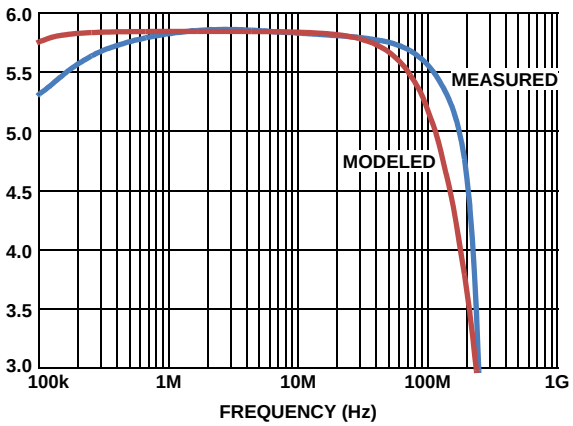

FIGURE 5. ADT4-6T RESPONSE CURVES

The measured curve is showing about -0.5dB at 100kHz and -0.3dB at 100MHz. The Spice model (used in subsequent simulations) is only attempting to match the high and low F_{-3dB} frequencies and the midband gain including the measured 0.2dB insertion loss. That modeling approach is described in this article: “Measuring and modeling wideband baluns for application to ADC input stages”
http://www.planetanalog.com/author.asp?section_id=434&doc_id=558824&

For a higher frequency range design, the MA/COM MABA-0096-CF48A0 measures in the same configuration to have a -0.5dB flatness span from 300kHz to 220MHz typically which would make it a good choice for 1MHz to 200MHz analog input span.

The ADT1-12 common mode choke following this actually has 0dB insertion loss in this configuration at low frequencies. This increases to -0.2dB midband with a -1dB point at >1GHz with these higher 200Ω source and load impedances used at this point in the signal chain.

The amplifier will have its own frequency response from these source impedances and gain settings. Having good simulation models for each of the elements in the design allow easy comparisons of options. Setting up an iSim PE circuit for the input stage of Figure 4 gives a simulation circuit of Figure 6.

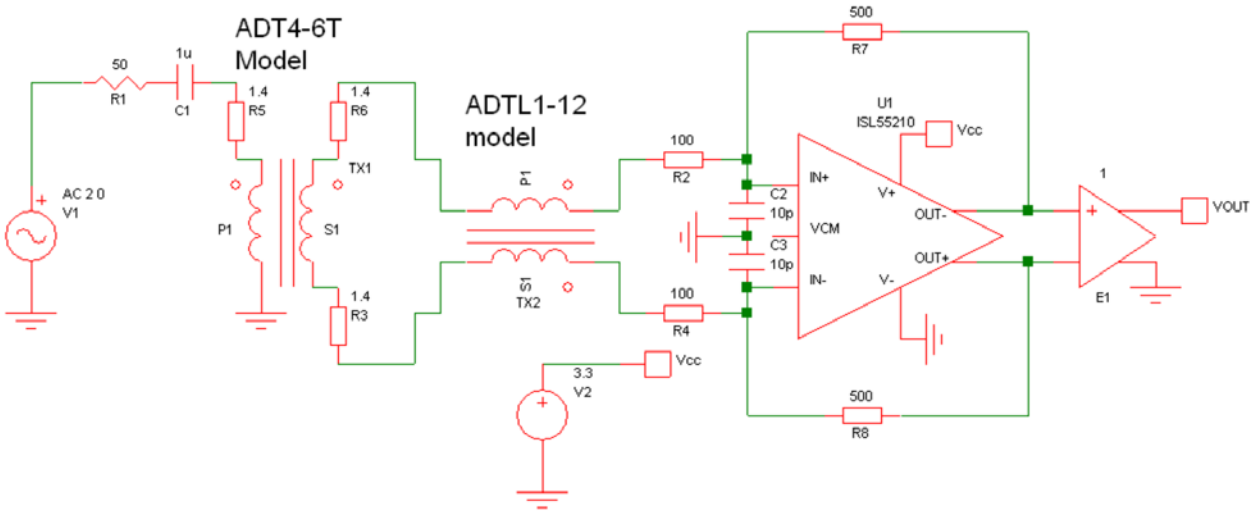

FIGURE 6. SIMULATION CIRCUIT FOR THE INPUT STAGE PART OF THE ISLA214P50-55210EV1Z BOARD

This is set up with the source V1 at a “2” amplitude to generate the response from the input to C1 to V_{OUT} as shown in Figure 7. The amplifier circuit is expecting a 50Ω source impedance for best flatness. The extrinsic one shown in Figure 6 will produce a 6dB loss to the board input of Figure 4 but simulating with a source set to “2” will remove that matching loss from the V_{OUT} plot. The simulated response shows exceptional flatness down to 100kHz and about -1dB rolloff at 100MHz. That rolloff will be equalized a bit with a slight peaking in the interstage filter design.

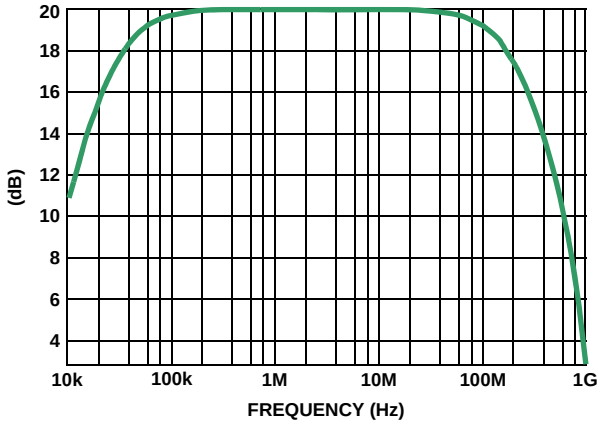

FIGURE 7. PREDICTED RESPONSE SHAPE TO V_{OUT} FOR A 50Ω SOURCE TO THE INPUT OF C1

INTERSTAGE FILTER FROM THE FDA OUTPUTS TO THE ADC

The signal path from the ISL55210 to the ADC is AC coupled, allowing the amplifier and ADC to operate at the common-mode voltage that optimize each device’s performance. As delivered, the differential output of the ISL55210 operate with a common mode voltage that is left to default to the internal 1.2V value. This can be adjusted to different set point via an optional path. The interstage passive circuit provides an AC coupled, 3rd order low pass filter. Built into this filter are an ADC common mode voltage servo loop which controls the common-mode DC voltage delivered to the ADC input pins and a wideband passive sense path going differential to single ended to directly measure the response shape to the ADC inputs. The circuit as delivered is shown in Figure 8.

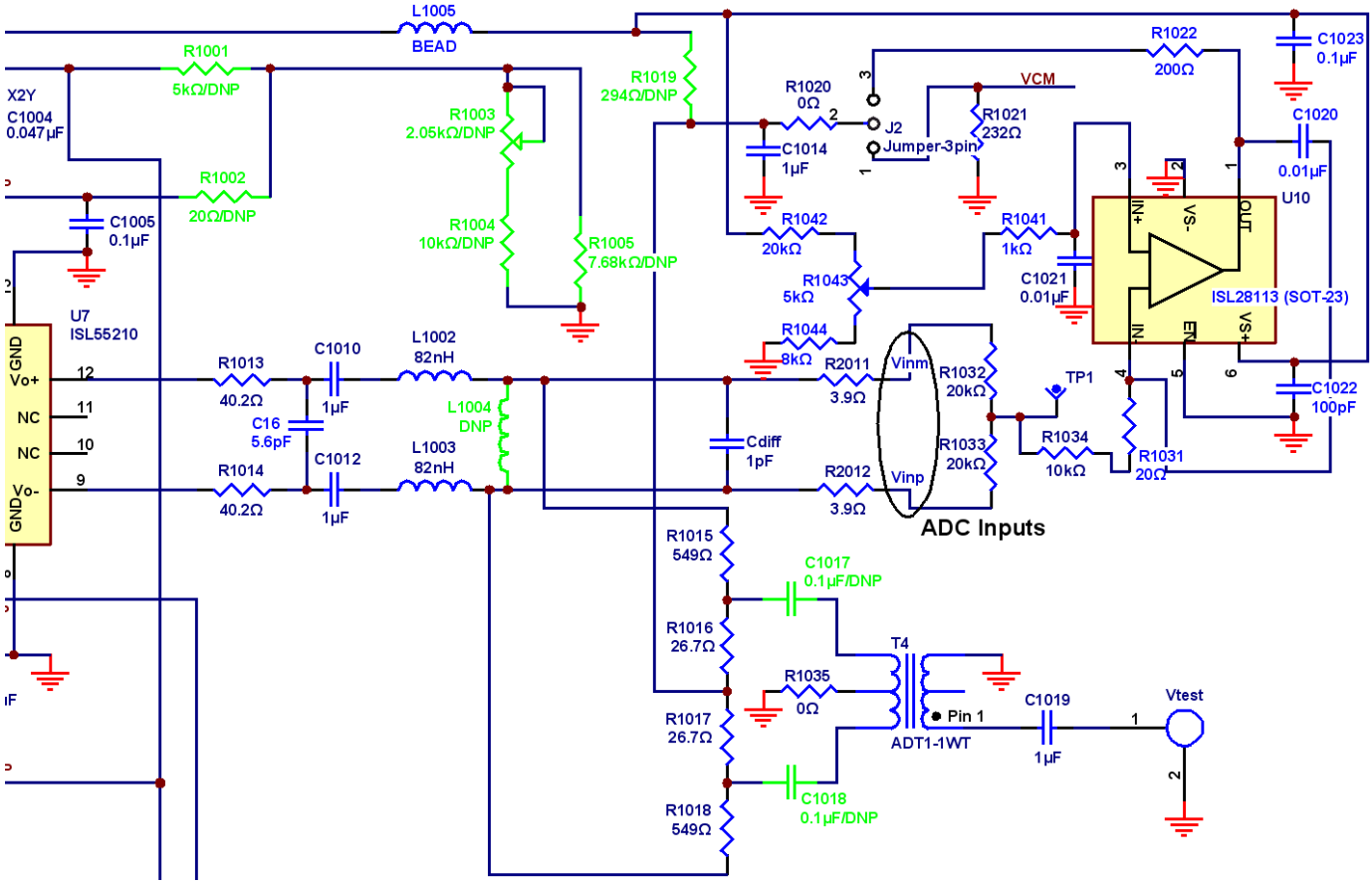

FIGURE 8. OUTPUT INTERFACE FROM ISL55210 TO THE ISLA214P50 DIFFERENTIAL INPUTS

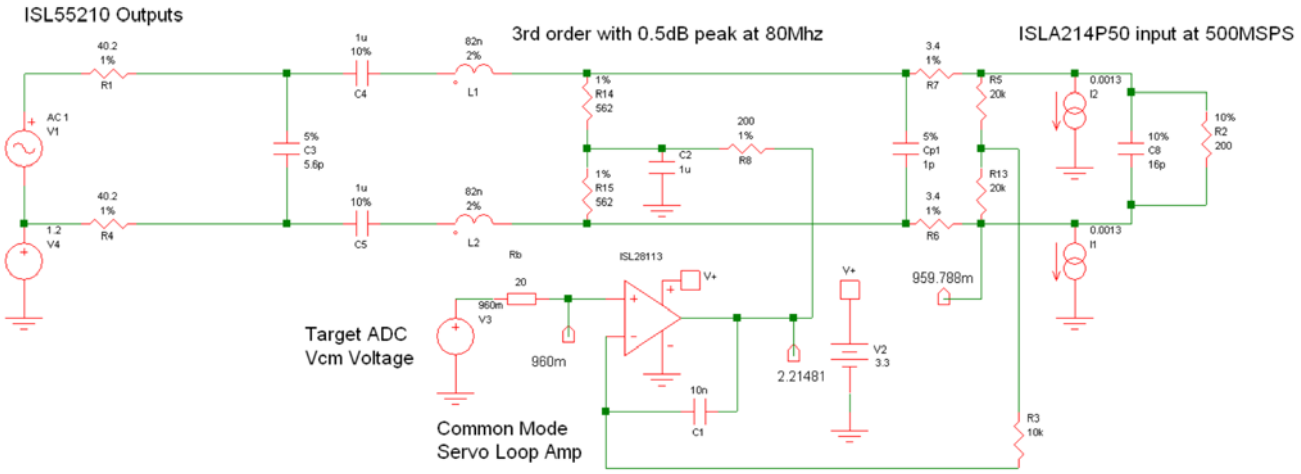

FIGURE 9. SIMULATION CIRCUIT FOR THE INTERSTAGE FILTER AND V_{CM} SERVO LOOP

Again, the green elements are optional and not populated. The non-populated elements connecting into C1005 would be the FDA V_{CM} adjustment if desired. As delivered, C1005 simply decouples the ISL55210 V_{CM} control pin which defaults internally to 1.2V on 3.3V supply. Not shown is a jumper on J2 from pin 2 to 3 to connect in the servo loop ADC V_{CM} control path. The ISLA214P50 ADC uses an unbuffered sample and hold and will therefore sink a sample rate dependent common-mode current which will give a sample rate dependent voltage drop from the midpoint of resistors R1015 – > R1018 and R2011, R2012. The servo loop is used primarily to counteract the sample-rate dependent voltage drop to deliver a fixed common-mode voltage to the ADC input pins across all sample clock rates. An alternate connection uses pin 2 to 1 on jumper J2 and populates R1019 to provide a fixed Thevenin source for the ADC V_{CM} control. This provides a simpler solution when the design is known to be a fixed clock rate design.

Numerous options exist for providing this ADC input V_{CM} voltage for different designs. The two offered on this board, along with several others, are detailed in this article: “Advantages to Precise Input Common Mode Voltage Control to High Performance High Speed ADC’s” http://www.edn.com/design/analog/4389814/Advantages-to-precise-input-common-mode-voltage-control-to-high-performance-high-speed-ADCs?page=0

The differential signal at the outputs of the ISL55210 proceeds from left to right in Figure 8 through the 40.2Ω resistors to a differential 5.6pF capacitor and then into the 1µF DC blocking capacitors. Those level shift the DC operating voltage from the FDA outputs to the required common mode voltage at the ADC inputs. The rest of the passive filter from there is pair of series 82nH inductors then into a parallel RC network comprised of the 4 resistor network feeding the differential to single ended sense path at the output of T4, an external 1pF differential capacitor and then the internal RC elements of the ADC. A final circuit element senses the average common mode voltage at the ADC inputs using the 2-20kΩ resistors and feeds that into a low frequency servo loop amplifier using the ISL28113 which then feeds a DC control voltage to the center of the 4-resistor string that acts to control the ADC common mode operating voltage to the reference voltage applied at the ISL28113 V+ input.

Critical to understanding the response shape are the estimated internal ADC elements as shown in the simulation circuit for this interface in Figure 9 (this element numbering here does not follow the build schematic of Figure 8)

At the far right the ADC is modeled as 2-clock rate dependent current sources (1.3mA here for the 500MSPS case) with an internal lumped element 16pF in parallel with 200Ω. The probes show the DC operating voltages where the 2.22V at the ISL28113 outputs gets back to the targeted 0.96V at the ADC inputs as those Icm currents pull down through the DC impedances from the output of the ISL28113. The internal ADC elements combine with the external RC elements to give the simulated frequency response shape from the ISL55210 outputs to the ADC inputs shown in Figure 10.

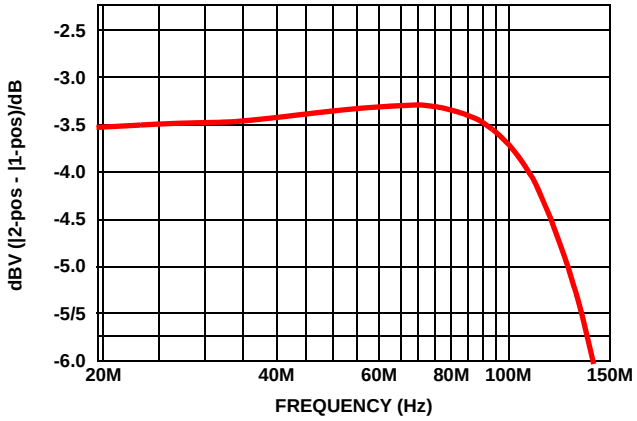

FIGURE 10. TARGETED RESPONSE SHAPE IN THE INTERSTAGE FILTER TO THE ADC

This slight peaking is intended to equalize some of the rolloff up to the FDA outputs but then bandlimit quickly above 100MHz. The V_{TEST} of Figure 8 provides an easy means to verify the frequency response shape from the board input to the ADC. The 4 resistor network feeding T4 in Figure 8 shows a about a 25Ω source to each leg of the 1:1 transformer while its total impedance across the signal path is part of the filter design. This path will have considerable insertion loss (≈-31.8dB) but an accurate replica of the response shape as shown for 2 boards measured in Figure 11.

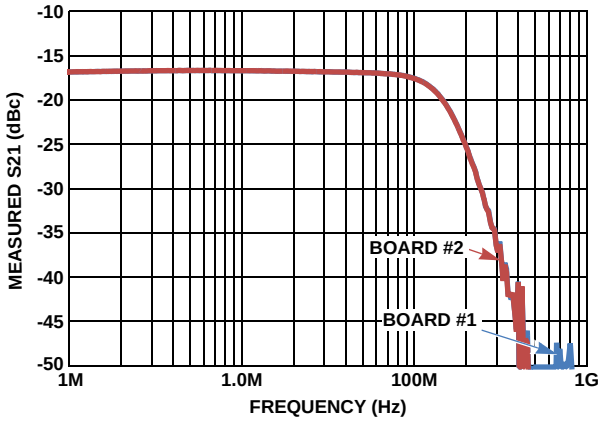

FIGURE 11. OVERALL FREQUENCY RESPONSE SHAPE FROM THE BOARD INPUT TO THE ADC

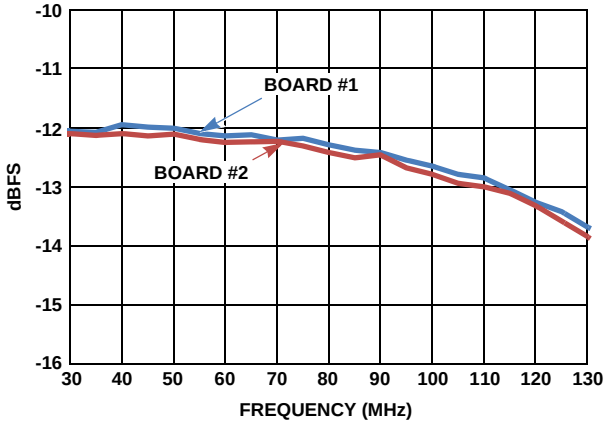

FIGURE 12. ZOOMED IN RESPONSE SHAPE USING THE ADC TO MEASURE FLATNESS

The ADC also can be used to measure the signal path frequency response by holding a constant input power while stepping the frequency and recording the change in the dBFS out of the FFT. This is shown on a linear frequency scale in Figure 12 targeting a single tone at -12dBFS out of the FFT at 30MHz, then holding constant input power and measuring the drop in dBFS as the frequency is stepped up.

Clearly the overall response shape is doing a good job of providing approximately 15dB gain from board edge with <-1dB rolloff to 100MHz. It is important for distortion reasons to stay away from the rolloff regions of the input step up transformer. The intended minimum frequency in this application is 100kHz, well above the 40kHz -1dB measured on t he ADT4-6T while the maximum intended frequency is 100MHz which is also well below the measured 180MHz -1dB frequency on the ADT4-6T. The interstage filter bandlimits the broadband noise out of the ISL55210 to reduce SNR degradation through the ADC while also providing a bit of HD2 and HD3 attenuation from the FDA outputs to the ADC inputs. For instance, a single tone 80MHz at the FDA output pins will have an HD2 at 160MHz and an HD3 at 240MHz. The response shape of Figure 11 suggests that HD2 term will get about 4dB attenuation while the HD3 term will get 13dB attenuation to the ADC inputs.

CLOCK AND CONTROL OPTIONS

The board offers several optional features that are in some cases not fully populated. The clock options and two other control inputs are shown in Figure 13.

The populated path for the ADC clock is the lower right input through the TC4-19G2 transformer. It is this path that must have a valid clock input (usually a filtered sine wave) when the Konverter software is started. Lab tests here were at 10dBm to 14dBm input levels at J4.

An alternate clock path is through an ADI – ADCLK905 differential output ECL clock driver. That path is populated by adding the SMA at the buffered clock input point at J5, adding the ECL clock buffer chip, populating the coupling caps (C46 and C47) and removing the coupling caps from the transformer input path (C28 and C29). This alternate clock path allows much lower power sine wave inputs into what is essentially a very low jitter differential output comparator. Its inputs are also differential, but one side is biased to the midpoint threshold to run single ended input. A very low phase noise sine wave inputs as low as -2dBm will generate the necessary output clock transition times to drive the ADC clock inputs. The clock chip includes internal 50Ω termination for the sine wave source.

A similar signal path is shown in Figure 13 just below the alternate clock path that provides an ADC sync operation if populated. To use this, add an SMA connector at J7 and the clock chip at U9. Refer to the ADC data sheet for the operation of this control path.

The amplifier may also be disabled through a high speed interface by populating the Pd SMA input through U5, a CMOS inverter. As delivered, the DC coupled 50Ω termination resistor holds the input at ground providing a 3.3V output to the disable control line on the ISL55210. This holds the amplifier in the enabled mode while connecting the SMA and driving that signal to a logic high, will disable the amplifier. It is important to recognize that even in the disable mode a signal path to the ADC will be present through the feedback resistors. It will be significantly attenuated from the active mode, but it will not be an open circuit. The ISL55210 includes two desirable features when disabled.

1. There are internal back to back diodes across the input summing junctions to limit the amplitude of high overdrive signals when disabled (or when active as well). In disable, this limits the maximum differential voltage available across the inputs to a diode voltage which is then all that can feed forward to the ADC – at an attenuated level.
2. A low power monitor circuit holds the output V_{CM} voltage at the same set point during disable as for the active mode. This prevents a long turn on time (or AC coupled common mode voltage spikes) through blocking caps in the output interface circuit as the amplifier cycles through enable/disable modes – further protecting the ADC from out of range inputs.

Contact the factory for assistance in exercising these clock and control options.

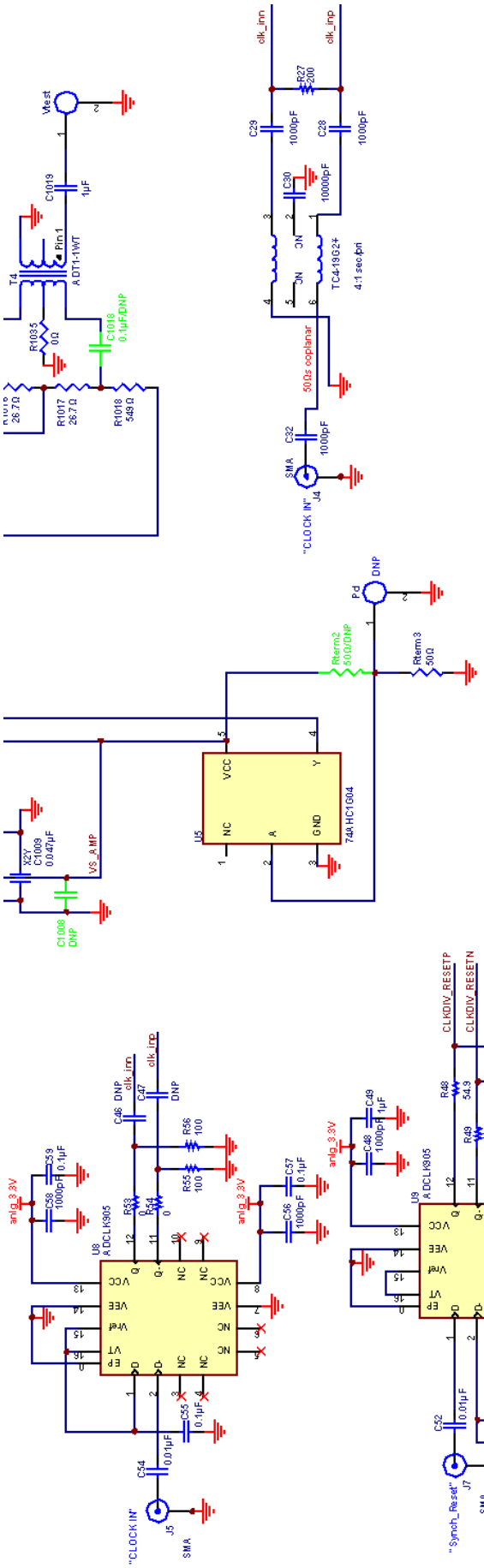

FIGURE 13. CLOCK AND CONTROL PORTION OF THE SIGNAL PATH SCHEMATIC

COMBINED FFT PERFORMANCE FOR THE INPUT INTERFACE CIRCUIT AND THE ADC

The starting point for the dynamic range of the ISLA214P50-55210EV1Z board would be the reported performance of the ADC only in its typical 2-transformer input evaluation board circuit. The typical ADC only EVM is described here:

http://www.intersil.com/content/dam/Intersil/documents/isla/isla214ir72ev1z_schem_layers.pdf

While the ISLA214P50 data sheet is available here: http://www.intersil.com/content/dam/Intersil/documents/fn75/fn7571.pdf

The SNR shown in Figure 2 from the ADC data sheet (and repeated here) is actually SNRFS.

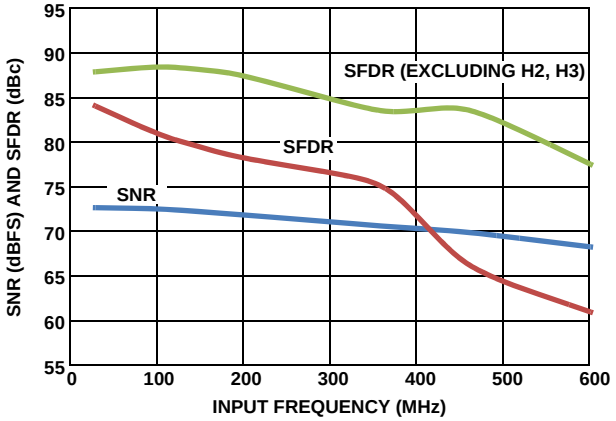

FIGURE 14. SNRFS AND SFDR vs F_{IN} USING 500MSPS CLOCK AND TARGETING -1dBFS

And then the swept frequency on just those HD2 and HD3 terms from Figure 3 in the ISLA214P50 data sheet.

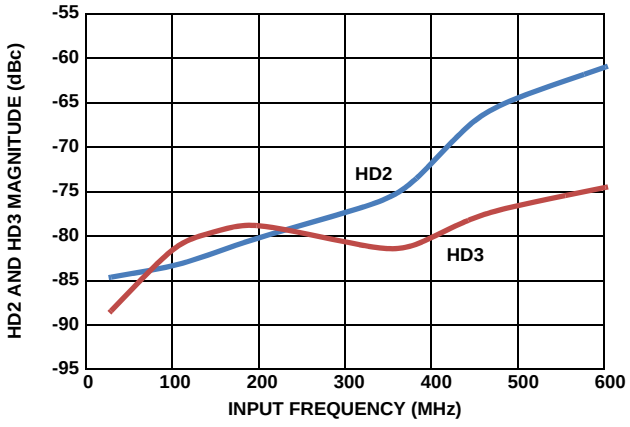

FIGURE 15. HD2 AND HD3 vs F_{IN} USING 500MSPS CLOCK AND TARGETING -1dBFS

Combining the information in these plots along with the specification table suggests the following typical numbers for the ADC only up through 100MHz inputs:

1. SNRFS ≈ 72.6dB
2. SFDR ≈ 82dBc to 84dBc
3. HD2 ≈< -84dBc
4. HD3 ≈< -80dBc

The SNRFS will certainly drop from this 72.6dB by some amount due to the added integrated noise presented to its inputs over a simple transformer input test. The HD2 and HD3 will show a complex result when combined with the ADC where that testing will be done here at -2dBFS. Recognizing that the midrange input frequencies will get little interstage filter help on the HD2 and HD3 terms, the 40MHz FFT of Figure 16 is showing that the intrinsic dynamic range up to the FDA outputs is so good as to produce almost no degradation in ADC only operation.

For this 283mV_{P-P} single tone input at 40.07MHz that is bandpass filtered and delivered to the SMA input, the:

1. SNRFS has dropped from 72.6dBc to 71.9dBc
2. SFDR is bit better than typical at 89dBc vs the ADC only 82dBc to 84dBc
3. HD2 has improved to -89dBc from ADC only of approximately -85dBc
4. HD3 has improved to -93dBc from a typical -88dBc looking at Figure 15 at 40MHz

Testing two boards for swept input frequency SNRFS gives the plot of Figure 17 where the result has dropped about 1dB from the ADC only data.

The swept frequency HD2 performance actually improves slightly over the ADC only plots. This might be attributed to the -2dBFS target but certainly shows no degradation using the very high dynamic range input interface circuit implemented on this board.

The swept frequency HD3 also seems slightly improved over the typical ADC only plots.

These plots are showing some degradation in SNRFS, and a slight improvement on the HD2 and HD3 performance. Here, however, the -2dBFS input level is only 283mV_{P-P} at board edge vs a much higher level for the typical ADC characterization circuit. The harmonic distortion performance is the combined result of many elements in the design. Hence, it is very difficult to make too strong a claim on the worst case distortion. The limited testing here seems to indicate a <-80dBc performance is certainly being delivered where even <-85dBc seems possible. While the signal path circuit here may seem a bit involved, it is converting from single ended input and delivering a bandlimited response to the ADC with precise common mode control and exceptionally low noise and distortion using <120mW total. Since the FFT's are showing nearly as good performance as the ADC itself, this solution is equivalent to a 14-bit, 500MSPS ADC requiring only 300mV_{P-P} single ended input for -1dBFS.

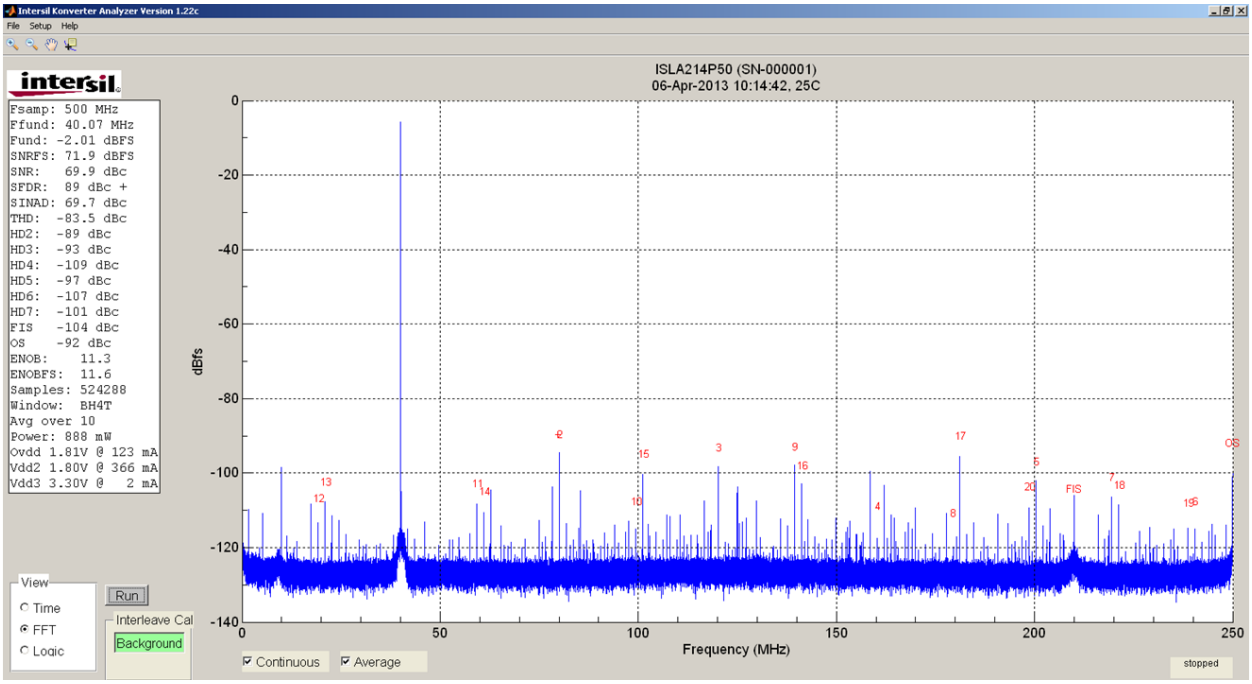

FIGURE 16. 40MHz INPUT, 500MSPS FFT FROM THE KONVERTER SOFTWARE

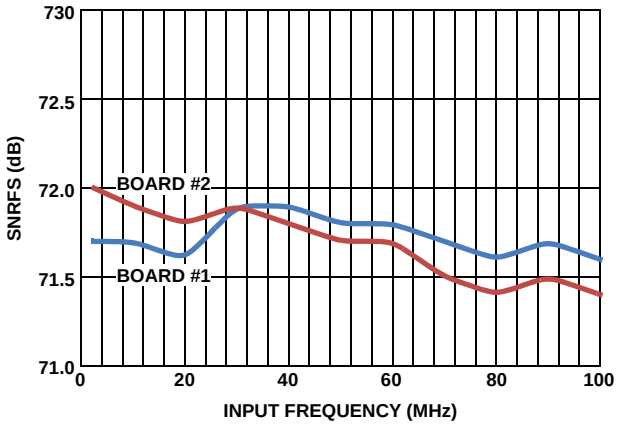

FIGURE 17. 500MSPS SNRFS RESULTS FOR 2 ISLA214P50-55210EV1Z BOARDS

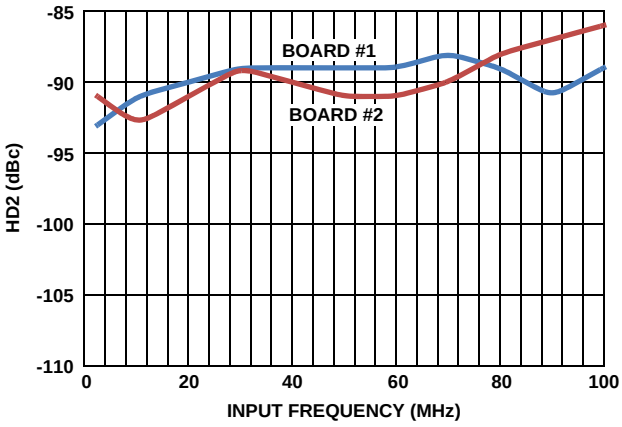

FIGURE 18. 500MSPS HD2 RESULTS FOR 2 ISLA214P50-55210EV1Z BOARDS

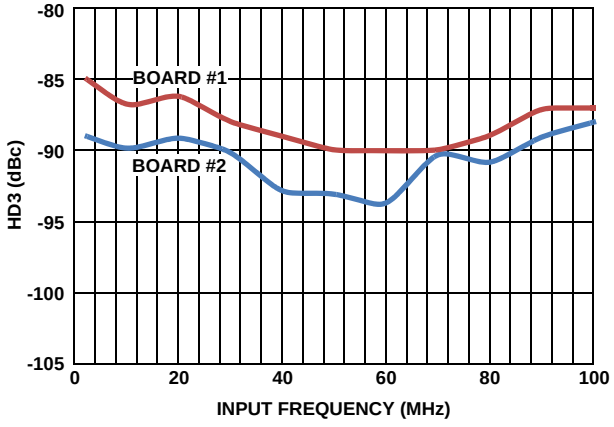

FIGURE 19. 500MSPS HD3 RESULTS FOR 2 ISLA214P50-55210EV1Z BOARDS

Tested Performance Over ADC Input V_{CM} Setting

Using the available ADC common mode voltage servo loop feature, it is an easy matter to move the DC operating voltage at the ADC inputs around and verify the range of good performance. Using the same basic targets of -2dBFs with a fixed Fin at 30MHz, one test board was swept from $0.9V_{CM}$ to $1.1V_{CM}$. The figure of merit here was the THD as the various spurious are moving around a lot with V_{CM} but the overall THD is relatively constant. Figure 20 shows this test at two clock frequencies.

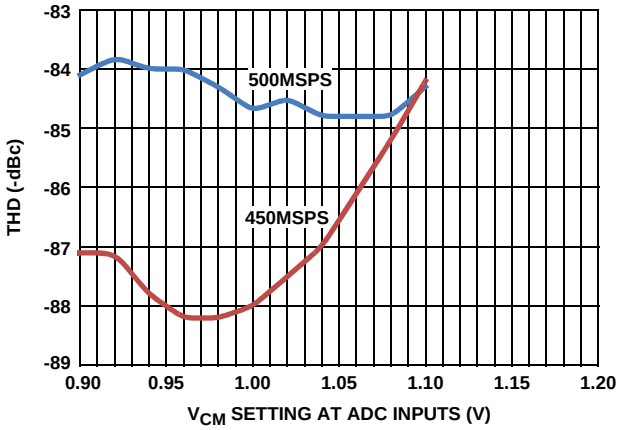

FIGURE 20. THD vs ADC INPUT COMMON MODE VOLTAGE

The 500MSPS data is relatively insensitive to V_{CM} input over this range showing very robust performance to varying V_{CM} input voltages. Overall improved spurious performance has been observed with this ADC at lower clock rates and the 450MSPS data shows a bit more sensitivity to the ADC input V_{CM} setting. In this test, the DC operating points through the FDA are not changing, none of the response shapes are changing up to the ADC, the only variable is the DC average input voltage for the signal being delivered to the ADC input pins. This is exercising fine scale input impedance nonlinearities in the ADC against the source impedance of the filter. While very robust over a relatively wide input V_{CM} range, the plot above suggested a $0.96V_{CM}$ set point for this board and that is the delivered condition. Changing the filter design and/or ADC might suggest a reset on that target ADC V_{CM} voltage. This is easily accomplished using the V_{CM} servo loop feature.

Tested Performance with Fixed F_{IN} and Narrow Clock Range Around 500MSPS

Since it seemed the FFT improved somewhat in dropping just below 500MSPS, a ±50MSPS range around 500MSPS was evaluated with a fixed 50MHz input generating a -2dBFS in the FFT. Looking again at the THD since the various spurious are moving around a lot with each test, gives the example performance of Figure 21.

This is indeed showing a pretty rapid improvement in THD dropping below 500MSPS and a good guardband above 500MSPS for acceptable performance. While it is not suggested that the ADC be operated above 500MSPS, this plot does show a good margin above that before catastrophic falloff in the THD. This is intended to add over temperature margin in the ADC performance.

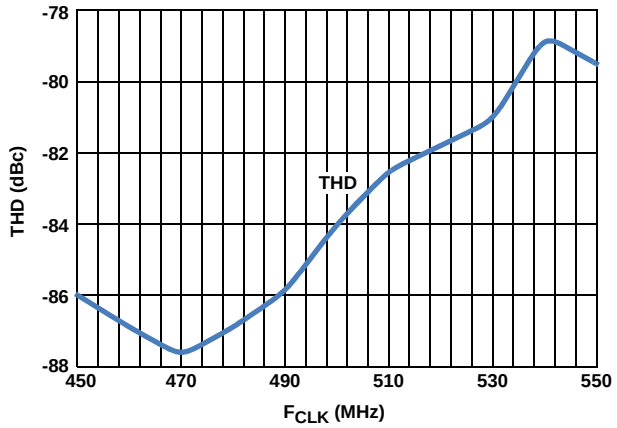

FIGURE 21. THD vs F_{CLK} AROUND THE 500MSPS SPECIFIED MAXIMUM CLOCK RATE

2-Tone, 3rd Order IM3 Testing

Since the board passes frequencies to 100MHz, duplicating the 70MHz IM3 performance reported in the ISLA214P50 data sheet will show the combined performance for the ADC and the interface circuit. The plot from the ISLA214P50 data sheet (Figure 16 there) is shown in Figure 22.

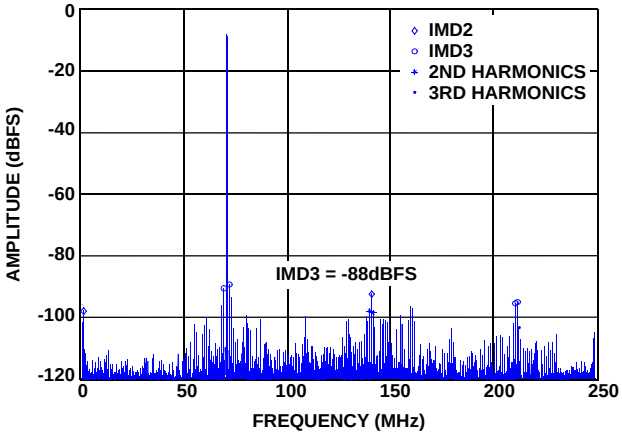

FIGURE 22. ISLA214P50 IM3 PLOT AT 70MHz AND 71MHz INPUTS FREQUENCIES

This is reporting a -88dBFS 3rd order intermodulation spurious for the 2 close in spurs at $\pm 3\Delta F_{IN}$ around the midpoint – that would be at 69MHz and 71MHz here. Converting this dBFS to dBc gives -80dBc for the IM3. For this broadband test, the IM2 is also apparent at 141MHz and 1MHz. Duplicating this set up with slightly lower carriers (-8dBFS vs -7dBFS on the ADC data sheet) at 69.5MHz and 70.5Mz gives the wideband FFT of Figure 23.

In this case, with 2 test tone inputs, the reported SNR does not compute correctly. It is easy to see here that the IM2 at 140MHz has been suppressed quite a lot by the combined excellent even order suppression in the interface circuit and the interstage filter. The other IM2 at 1MHz is also lower. Zooming in on a 65MHz to 75MHz range in Figure 24 shows exceptionally low 3rd order terms in this solution.

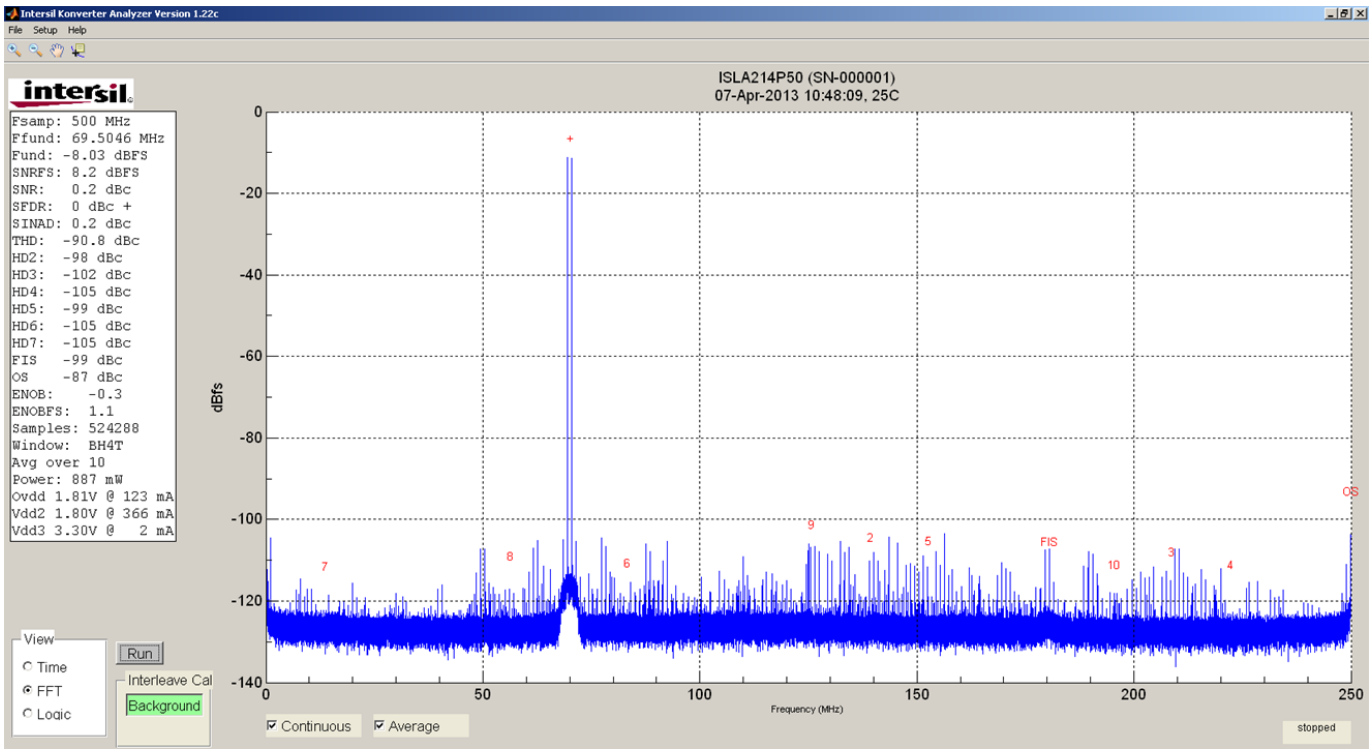

FIGURE 23. FULL NYQUIST SPAN FFT FOR A 70MHz IM3 TEST

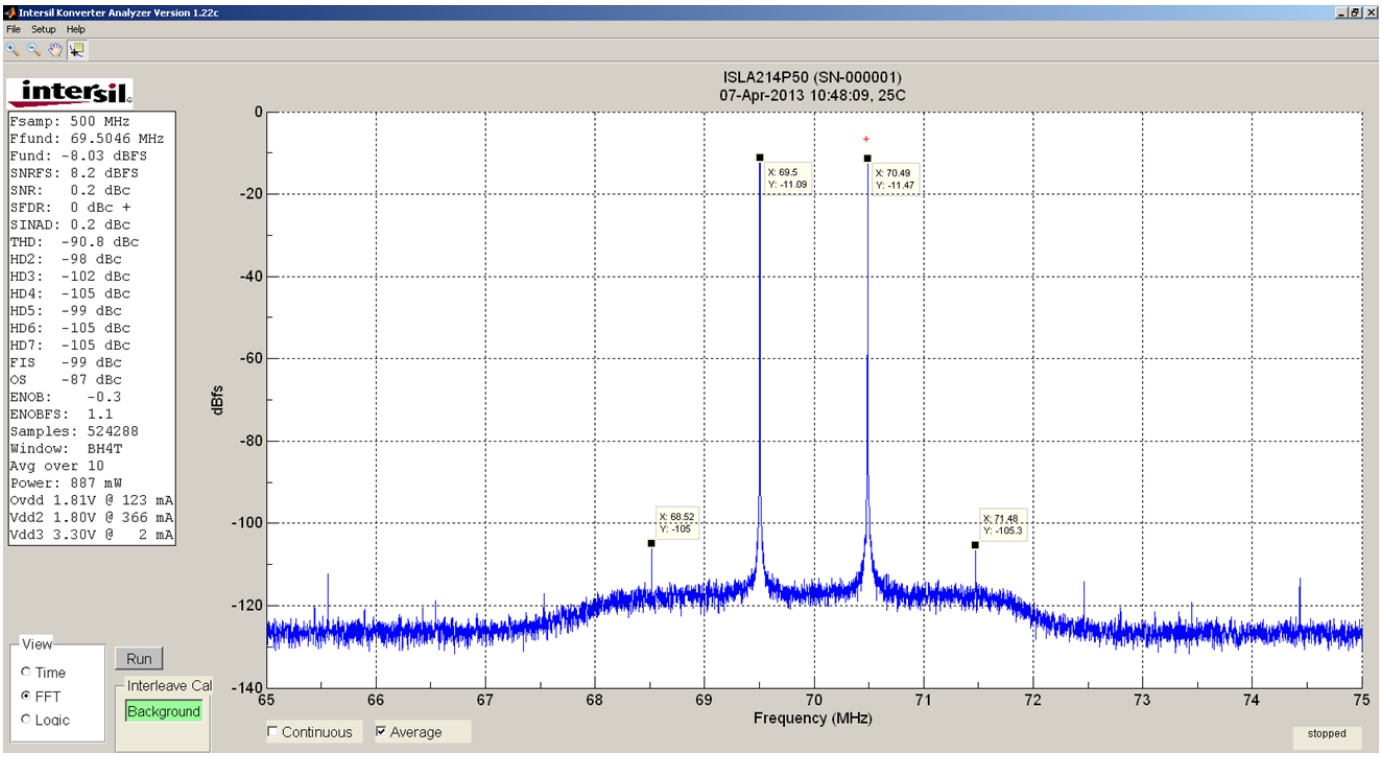

FIGURE 24. ZOOMED IN FFT AROUND THE CARRIER FREQUENCIES

The data markers are showing -11dBFS on the carriers and -105dBFS on the 3rd order intermodulation spurious terms. This is the raw data where the actual carriers were each -8dBFS and are reduced 3dB in the data by the 4-term Blackman Harris windowing being used. In any case this is showing ≈-94dBc IM3 performance at 70MHz. The bandpass filter shape can also be seen easily in the noise floor. This -94dBc far exceeds the ADC performance shown in Figure 22 which might be attributed to a lower spurious input test signal using the 15dB gain in front of the ADC here or perhaps poorer IM3 in the interface elements on the ADC only EVM board. The ISL55210 is very nearly un-measurable for OIP3 at 70MHz and that is clearly reflected in the significantly improved performance of Figure 24. Dropping the test power levels showed an intercept performance in the FFT where dropping only 3dBm on the two test powers dropped the spurious 9dB into the noise floor.

Appendix A: Low Phase Noise RF Generators

Some examples of low phase noise generators suitable for high resolution ADC clock and source signal generation in test include:

1. Rohde & Schwarz: SMA100A
2. Agilent 8664A
3. Gigatronics 6080A

For fixed 500MSPS clock operation, the Crystek RFPRO33-500.00 offers a simple solution. This device operates within an SMA body and requires a 3.3V supply to produce the required clock to operate this EVM. Bandpass filtering on the clock always helps the SNR performance for any of these sources. Most of the data here was taken with the 8664A which seemed to give the best SNRFS results.

TESTED PERFORMANCE OVER A WIDE RANGE OF CLOCK FREQUENCY AND FIN

As the clock rate is reduced several slight changes in the response can be expected.

1. The Icm current into the 2 ADC inputs will decrease. Using the servo loop amplifier will act to hold the ADC input V_{CM} voltage constant as the clock rate is changed.
2. The ADC input resistance will increase slightly. The 200Ω internal value shown in the simulation circuit of Figure 9 is a combination of an extrinsic 300Ω element and the effective resistance of a sampling cap. That impedance is approximately 1/(Fs*3.3pF). As the clock rate decreases, this impedance will increase moving the apparent input resistance up. By 200MSPS the total ADC internal resistance is ≈250Ω. This shift will slightly change the response shape of the interstage filter.
3. Reducing the clock rate gives every operation internal to the ADC a bit more time to settle and improved dynamic range over the analog input frequency is observed.

The following figures summarize the swept input frequency dynamic range vs Fsample repeating the 500MSPS data for comparison to 450MSPS. These are all targeting a -2dBFS using very low phase noise sources and bandpass filtering on both the clock and Fin. In general, at clock rates ≤450MSPS the HD2 and HD3 terms hold below -85dBc.

500MSPS

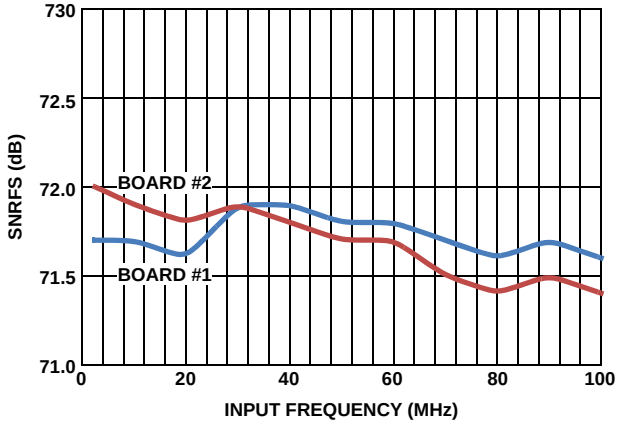

FIGURE 25. 500MSPS SNRFS

450MSPS

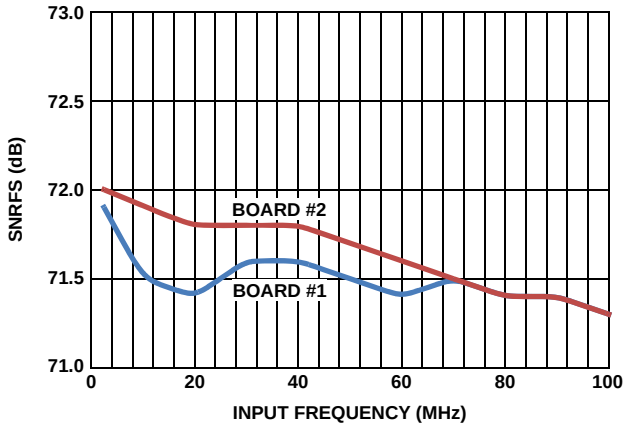

FIGURE 26. 450MSPS SNRFS

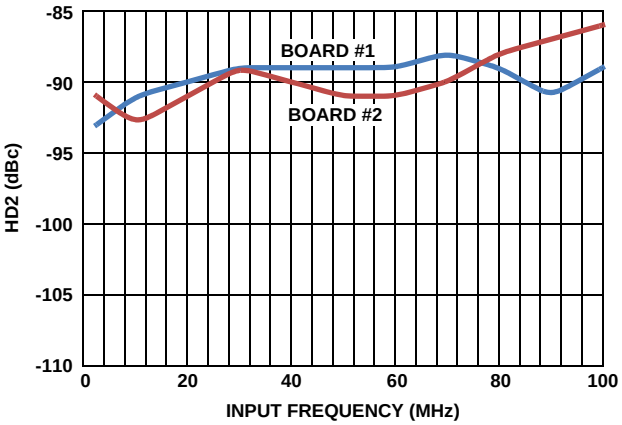

FIGURE 27. 500MSPS HD2

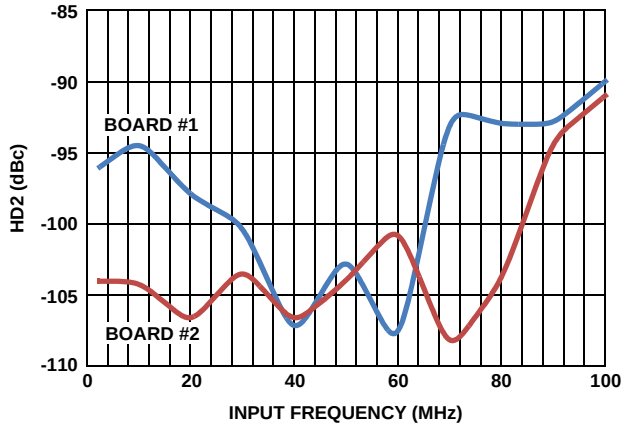

FIGURE 28. 450MSPS HD2

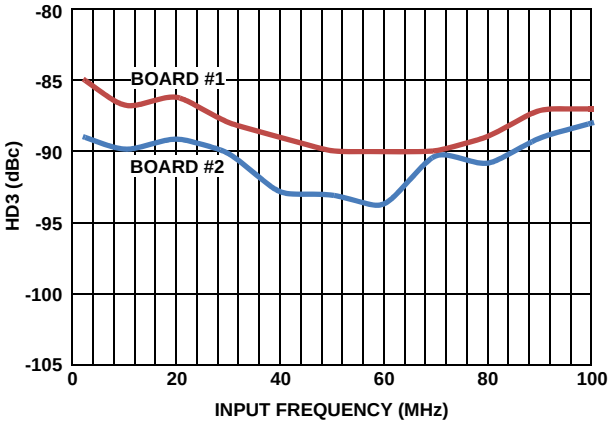

FIGURE 29. 500MSPS HD3

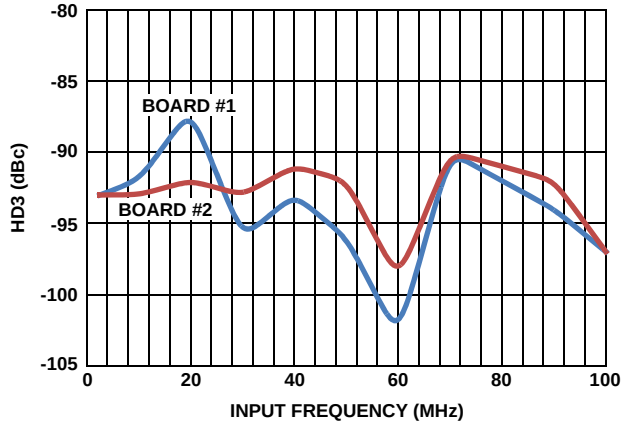

FIGURE 30. 450MSPS HD3

400MSPS

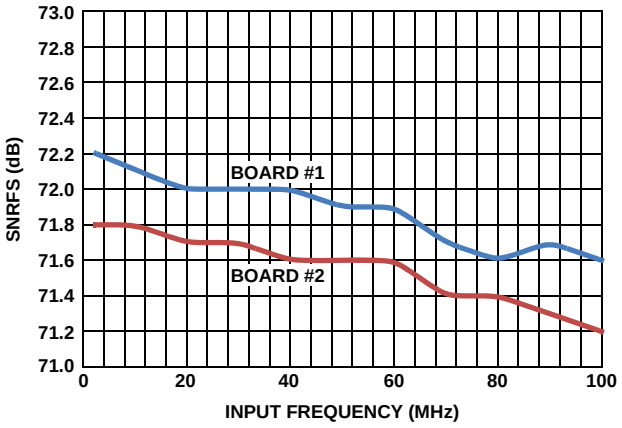

FIGURE 31. 400MSPS SNRFS

350MSPS

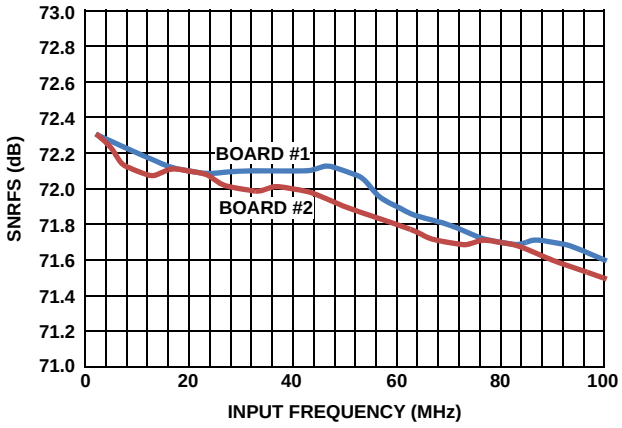

FIGURE 32. 350MSPS SNRFS

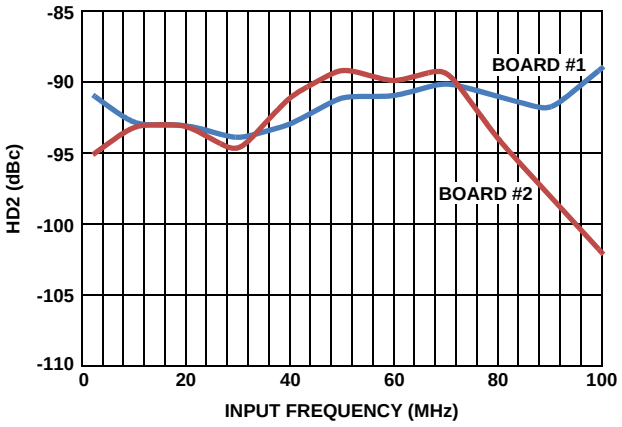

FIGURE 33. 400MSPS HD2

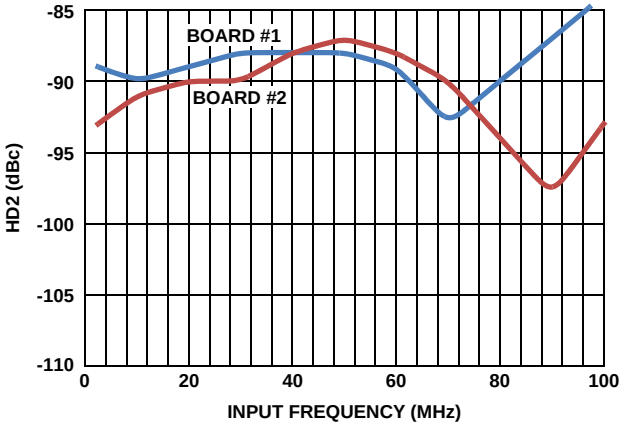

FIGURE 34. 350MSPS HD2

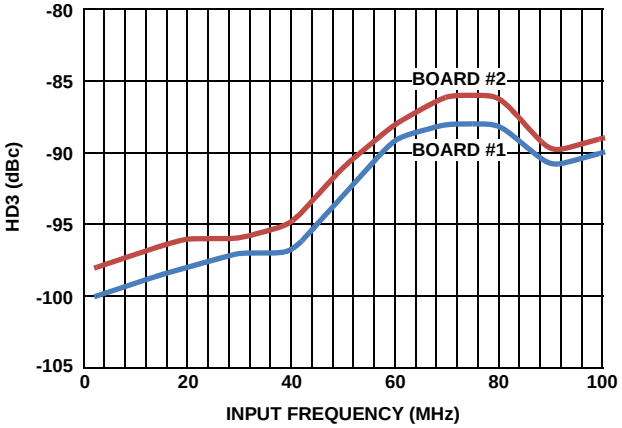

FIGURE 35. 400MSPS HD3

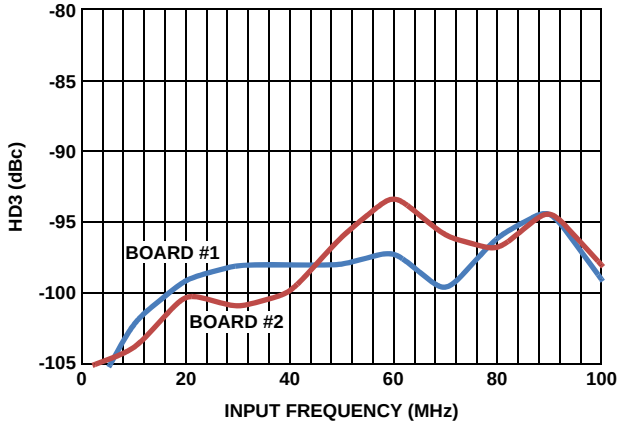

FIGURE 36. 350MSPS HD3

300MSPS

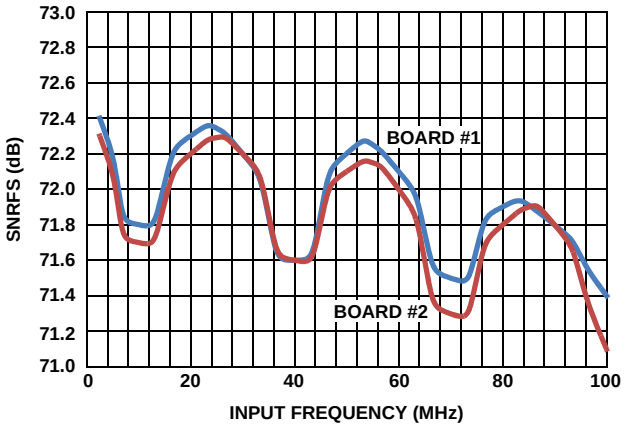

FIGURE 37. 300MSPS SNRFS

250MSPS

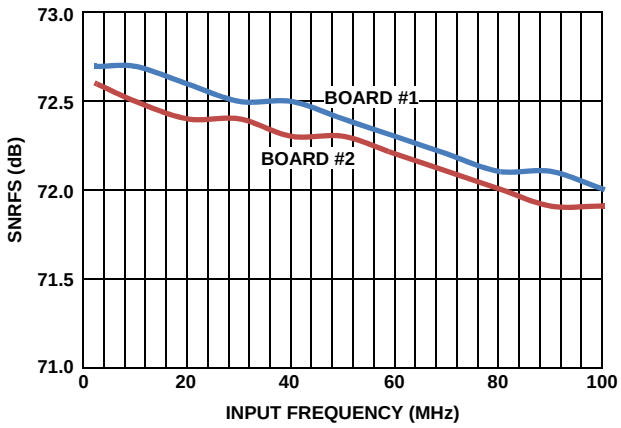

FIGURE 38. 250MSPS SNRFS

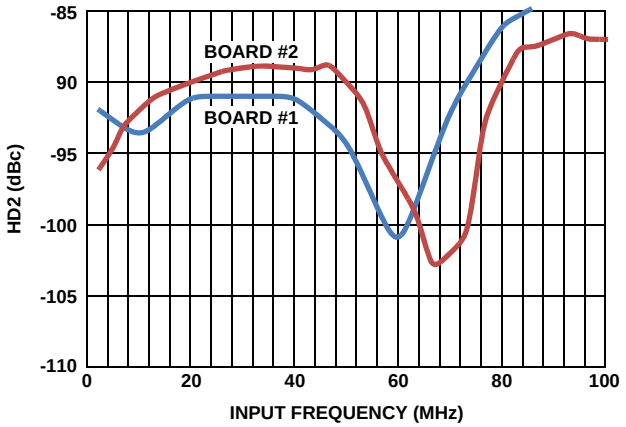

FIGURE 39. 300MSPS HD2

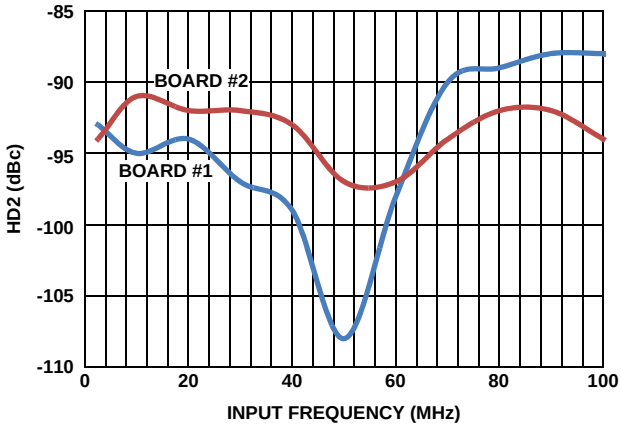

FIGURE 40. 250MSPS HD2

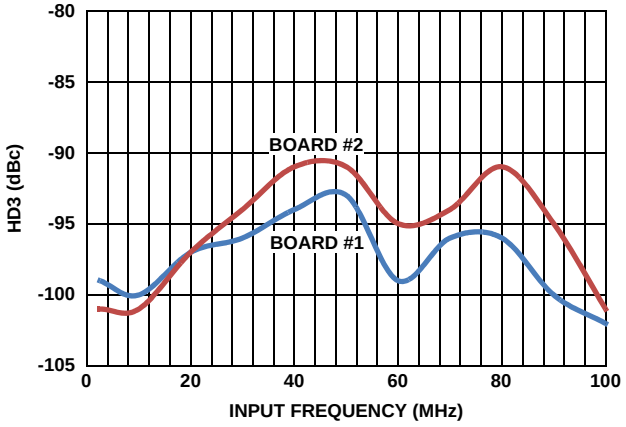

FIGURE 41. 300MSPS HD3

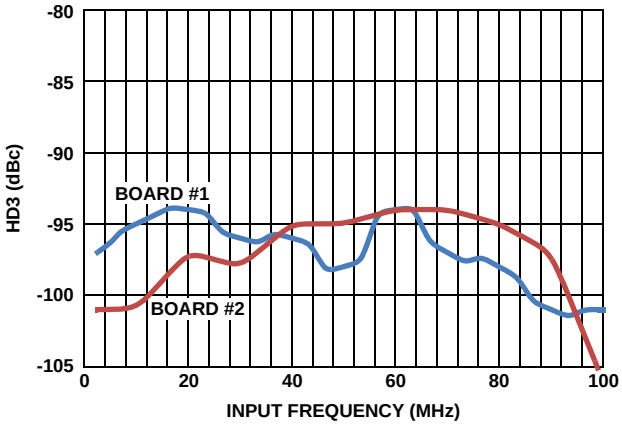

FIGURE 42. 250MSPS HD3

200MSPS

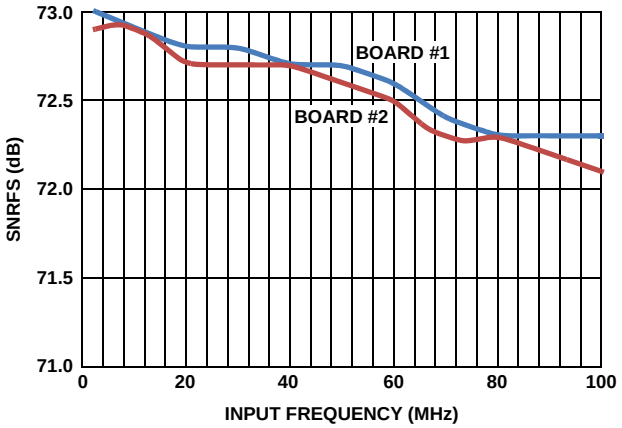

FIGURE 43. 200MSPS HD2

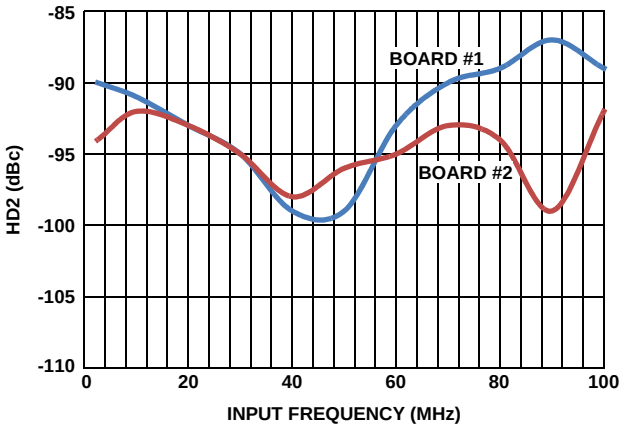

FIGURE 44. 200MSPS HD2

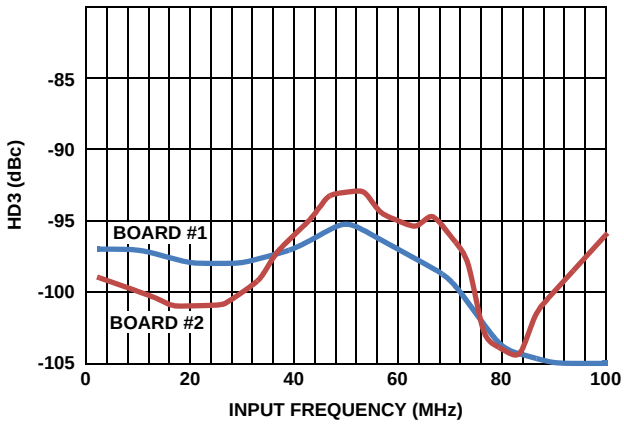

FIGURE 45. 200MSPS HD3

Board Options

While this board shows a complete example of a low power, high dynamic range, single to differential amplifier stage, numerous options can be implemented on this board. Principally, the gain in the amplifier can be easily changed modifying the feedback resistors up or down (R1008, R1011). The output filter can be re-designed for a different passband. L1004 is included (Figure 8) to implement bandpass filters on this board as well.

The ISLA214P50 is part of a large pin compatible ADC family. Those can be dropped into this board replacing the ISL214P50 but will require some redesign in the filter for different ADC input impedances and a reprogramming through the Konverter software for the specific ADC. Contact the factory for assistance with this. Table 2 summarizes the pin compatible, high performance, ADC family supported by this single daughtercard. These span a large range in bits and maximum clock rate where lower clock rates run lower power in each family of devices.

TABLE 2. PIN COMPATIBLE HIGH PERFORMANCE ADC FAMILY

PART NUMBER	RESOLUTION (Bits)	MAXIMUM SAMPLE RATE (Msps)	POWER CONSUMPTION (mW)
ISLA216P25	16	250	785
ISLA216P20	16	200	720
ISLA216P13	16	130	615
ISLA214P50	14	500	835/900 (Note)
ISLA214P25	14	250	450
ISLA214P20	14	200	410
ISLA214P13	14	130	360
ISLA214P12	14	125	310
ISLA212P50	12	500	823/892 (Note)
ISLA212P25	12	250	440
ISLA212P20	12	200	405
ISLA212P13	12	130	355

NOTE: I2E disabled/enabled.

Full Signal Path Schematic

The full schematic from input to ADC pins is shown in Figure 46.

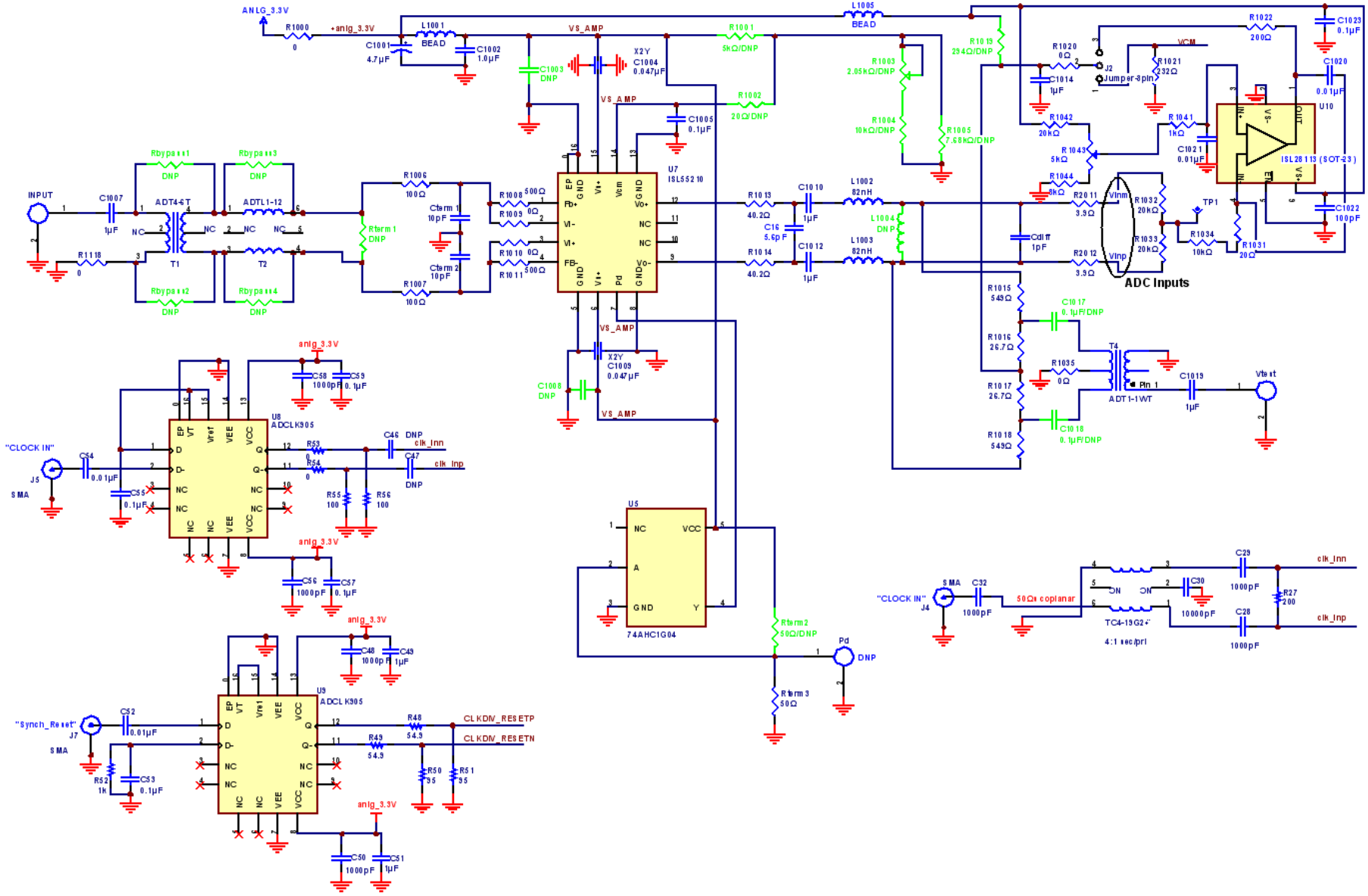

FIGURE 46. FULL SIGNAL PATH SCHEMATIC

The following BOM is for the entire ISLA214P50-55210EV1Z board. It includes some elements not described here that are associated with the ADC operation common to its EVM board – the ISLA214P50IR72EV1Z. The main focus of this board is to add a very high linearity input interface circuit that has been thoroughly described here. Elements in the following BOM that do not have a description in the comments column are not part of the signal path but common to the ADC only EVM board.

ISLA214P50-55210EV1Z Bill of Materials ☐ Shaded rows unpopulated

PART NUMBER	QTY	UNITS	REFERENCE DESIGNATOR	COMMENT	DESCRIPTION	MFR.	MFR. PART
ISLA214P50-55210EZRVBPCB	1	ea		Blank Board	PWB-PCB, ISLA214P50-55210EZ, REVB, ROHS	IMAGINEERING INC	ISLA214P50-55210EZRVBPCB
160X14W473MV4T-T	2	ea	C1004, C1009	ISL55210 supply decoupling	CAP-X2Y, SMD, 0603, 0.047µF, 16V, 20%, X7R, ROHS	JOHANSON DIELECTRICS INC	160X14W473MV4T
GRM188R71E105KA12D-T	4	ea	C1007, C1010, C1012, C1019	Signal path blocking caps	CAP, SMD, 0603, 1µF, 25V, 10%, X7R, ROHS	MURATA	GRM188R71E105KA12D
H1044-00100-50VR25-T	2	ea	Cterm1, Cterm2	Response shaping at inverting summing junctions	CAP, SMD, 0402, 10pF, 50V, 0.25pF, NP0, ROHS	AVX	04025U100CAT2A
H1044-00101-50V5-T	1	ea	C1022	ISL28113 supply decoupling cap	CAP, SMD, 0402, 100pF, 50V, 5%, C0G, ROHS	MURATA	GRM1555C1H101JZ01D
H1044-00102-16V10-T	4	ea	C28, C29, C48, C58	ADCLK905 supply decoupling & ADC transformer clock path	CAP, SMD, 0402, 1000pF, 16V, 10%, X7R, ROHS	TDK	C1005X7R1C102K
H1044-00103-16V10-T	3	ea	C30, C1020, C1021	Vcm servo loop caps around ISL28113 & clock transformer centertap AC gnd	CAP, SMD, 0402, 0.01µF, 16V, 10%, X7R, ROHS	TDK	C1005X7R1C103K
H1044-00104-16V10-T	17	ea	a) C4, C5, C20, C22, C24, C27, C33, C34, C42	Various supply decoupling caps, largely on the bottom of the board.	CAP, SMD, 0402, 0.1µF, 16V, 10%, X7R, ROHS	VENKEL	C0402X7R160-104KNE
H1044-00104-16V10-T	0	ea	b) C43, C44, C45, C50, C56, C113, C114, C115	Various supply decoupling caps, largely on the bottom of the board.	CAP, SMD, 0402, 0.1µF, 16V, 10%, X7R, ROHS	VENKEL	C0402X7R160-104KNE
H1044-00105-10V10-T	1	ea	C1014	Vcm feedback point decoupling cap.	CAP, SMD, 0402, 1.0µF, 10V, 10%, X5R, ROHS	MURATA	GRM155R61A105KE15D
H1044-005R6-50VR5-T	1	ea	C16	3rd order interstage differential filter cap	CAP, SMD, 0402, 5.6pF, 50V, 0.5pF, NP0, ROHS	MURATA	GRM1555C1H5R6DZ01D
H1044-DNP	0	ea	a) C8, C9, C10, C11, C12, C13, C14, C15		CAP, SMD, 0402, DNP-PLACE HOLDER, ROHS		
H1044-DNP	0	ea	b) C25, C35-C38, C46, C47	Optional clock and control signal path caps not populated	CAP, SMD, 0402, DNP-PLACE HOLDER, ROHS		
H1045-00010-50VR1-T	1	ea	Cdiff	3rd order interstage differential filter cap	CAP, SMD, 0603, 1.0pF, 50V, 0.1pF, NP0, ROHS	TDK	C1608C0G1H010B
H1045-00102-50V10-T	1	ea	C32	Clk input to transformer	CAP, SMD, 0603, 1000pF, 50V, 10%, X7R, ROHS	AVX	06035C102KAT2A
H1045-00103-16V10-T	2	ea	C52, C54	ADCLK905 input signal coupling	CAP, SMD, 0603, 0.01µF, 16V, 10%, X7R, ROHS	VENKEL	C0603X7R160-103KNE

ISLA214P50-55210EV1Z Bill of Materials ☐ Shaded rows unpopulated (Continued)

PART NUMBER	QTY	UNITS	REFERENCE DESIGNATOR	COMMENT	DESCRIPTION	MFR.	MFR. PART
H1045-00104-25V10-T	6	ea	C2, C3, C53, C55, C1005, C1023	Various supply and bias line decoupling caps.	CAP, SMD, 0603, .1µF, 25V, 10%, X7R, ROHS	MURATA	GRM39X7R104K025AD
H1045-00105-50V10-T	4	ea	C49, C51, C57, C59	Supply decoupling on the ADCLK905's	CAP, SMD, 0603, 1µF, 50V, 10%, X5R, ROHS	TDK	C1608X5R1H105K
H1045-DNP	0	ea	C1003, C1008, C1017, C1018	Alternate ISL55210 supply decoupling & Vtest path coupling	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS		
H1065-00105-16V10-T	1	ea	C1002	Main 3.3V supply line decoupling	CAP, SMD, 1206, 1µF, 16V, 10%, X7R, ROHS	PANASONIC	ECJ-3FB1C105K
H1112-00336-16V10-C-T	4	ea	C1, C6, C7, C31	Supply decoupling	CAP-TANT, SMD, C, 33µF, 16V, 10%, ROHS	AVX	TAJC336K016RNJ
H1121-00475-10V10-B-T	1	ea	C1001	3.3V supply decoupling to ISL55210	CAP-TANT, LOW ESR, SMD, B, 4.7µF, 10V, 10%, 3.5Ω, ROHS	KEMET	T491B475K010AT
0603CS-82NXGLU	2	ea	L1002, L1003	Signal path 3rd order filter inductors	COIL-RF INDUCTOR, SMD, 0603, 82nH, 2%, 400mA, ROHS	COILCRAFT	0603CS-82NXGLU
142-0701-851	1	ea	INPUT	Analog input signal end launch SMA	CONN-RF, SMA JACK, 50Ω, BMT, TAB-END LAUNCH, ROHS	JOHNSON COMPONENTS	142-0701-851
22-28-4360-1X3	1	ea	J2	Jumper to select ADC Vcm set path, defaulted to use the servo loop with pins 2 & 3 shorted.	CONN-HEADER, 1X3, BRKAWY-1X36, 2.54mm, 0.240X0.125, ROHS	MOLEX	22-28-4360
5002	1	ea	TP1	Sense point for average CM at ADC input pins	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	KEYSTONE	5002
5004	1	ea	Amplifier +3.3V	Sense point for the 3.3V supply to the signal path amplifier	CONN-MINI TEST POINT, VERTICAL, YEL, ROHS	KEYSTONE	5004
5011	1	ea	GND	GND connector tap into for setting Vcm voltage with DVM	CONN-MULTI-PURPOSE TEST PT, BLK, ROHS	KEYSTONE	5011
55091-1875	1	ea	J6	Mezzanine connector on board bottom to mate to motherboard	CONN-HEADER, SMD, DUAL ROW, 180P, 0.635PITCH, 6mmSTACK, ROHS	MOLEX	55091-1875
70280-0458-2X2	2	ea	JP1, JP2	Headers to select ADC options. Only JP1 is used with jumper connected set of pins closer to Input	CONN-HEADER, 2X2, BRKAWY-2X50, 2.54mm, ROHS	MOLEX	70280-0458
87832-1420	1	ea	J1	CPLD connector	CONN-HEADER, SHROUDED, SMD, 14P, 2mmPITCH, CENTER SLOT, ROHS	MOLEX	87832-1420

ISLA214P50-55210EV1Z Bill of Materials ☐ Shaded rows unpopulated (Continued)

PART NUMBER	QTY	UNITS	REFERENCE DESIGNATOR	COMMENT	DESCRIPTION	MFR.	MFR. PART
901-144-8RFX	1	ea	J4	default clock input SMA to XFMR path	CONN-RF, SMA JACK, 50Ω, PCB MNT, STRAIGHT, ROHS	AMPHENOL	901-144-8RFX
SPC02SYAN	2	ea	JP1-Pins 3-4, J2-Pins 2-3.	Connecting jumpers on the JP1 and J2 posts	CONN-JUMPER, SHORTING, 2PIN, BLACK, GOLD, ROHS	SULLINS	SPC02SYAN
HZ1206E601R-10-T	2	ea	L1001, L1005	+3.3V supply line ferrites to ISL55210 and ISL28113	FERRITE-EMI CHIP, SMD, 1206, 600Ω, 500mA, ROHS	LAIRD TECHNOLOGIES	HZ1206E601R-10
MMZ2012R102A-T	14	ea	L3, L4, L8, L10-L20		FERRITE BEAD, SMD, 0805, 1k, 0.5A, 100MHz, ROHS	TDK	MMZ2012R102A
24FC128-I/SN	2	ea	U2 U3	Back side components	IC-I2C SERIAL EEPROM, 8P, SOIC, 128 KBIT, ROHS	MICROCHIP TECHNOLOGY	24FC128-I/SN
ISL28113FHZ	1	ea	U10	ADC Vcm control servo loop op amp	IC-RRIO OP AMP, 5P, SOT-23-5, ROHS	INTERSIL	ISL28113FHZ
ISL55210IRTZ	1	ea	U7	Signal path fully differential amplifier	IC-DIFFERENTIAL AMP, 16P, TQFN, 3X3, ROHS	INTERSIL	ISL55210IRTZ
ISLA214P50IRZ	1	ea	U1	ADC	IC-14-BIT, 500MSPS A/D CONVERTER, 72P, QFN, 10X10, ROHS	INTERSIL	ISLA214P50IRZ
SN74AHC1G04DBVR-T	1	ea	U5	ISL55210 disable control line inverter	IC-SINGLE INVERTER GATE, 2V-5.5V, 5P, SOT-23-5, ROHS	TEXAS INSTRUMENTS	SN74AHC1G04DBVR
XC2C64A-7VQG44C	1	ea	U4		IC-CR-II CPLD, SMD, 44P, VQFP, 64MACROCELLS, 10X10, ROHS	XILINX	XC2C64A-7VQG44C
3299W-1-502LF	1	ea	R1043	ADC Vcm adjust pot	POT-TRIM, TH, 5k, 0.5W, 10%, 3P, 3/8, ROHS	BOURNS	3299W-1-502LF
H2510-00200-1/16W1-T	1	ea	R1031	Isolating resistor into ISL28113 summing junction	RES, SMD, 0402, 20Ω, 1/16W, 1%, TF, ROHS	PANASONIC	ERJ2RKF20R0
H2510-003R9-1/16W1-T	2	ea	R2011, R2012	Kickback isolation at ADC input pins	RES, SMD, 0402, 3.9Ω, 1/16W, 1%, TF, ROHS	VISHAY/DALE	CRCW04023R90FKED
H2510-00R00-1/16W-T	7	ea	R53, R54, R1009, R1010, R1118, R1020, R1035	Various shorting paths in signal path circuit	RES, SMD, 0402, 0Ω, 1/16W, 5%, TF, ROHS	VENKEL	CR0402-16W-00T
H2510-01000-1/16W1-T	4	ea	R55, R56, R1006, R1007	Input termination & gain elements, and ADCLK905 output load	RES, SMD, 0402, 100Ω, 1/16W, 1%, TF, ROHS	VENKEL	CR0402-16W-1000FT
H2510-01001-1/16W1-T	21	ea	a) R1, R4-R13, R30, R36, R38, R42, R52, R57,		RES, SMD, 0402, 1k, 1/16W, 1%, TF, ROHS	VENKEL	CR0402-16W-102JT
H2510-01001-1/16W1-T	0	ea	b) R58, R59, R60, R1041.		RES, SMD, 0402, 1k, 1/16W, 1%, TF, ROHS	VENKEL	CR0402-16W-102JT

ISLA214P50-55210EV1Z Bill of Materials ☐ Shaded rows unpopulated (Continued)

PART NUMBER	QTY	UNITS	REFERENCE DESIGNATOR	COMMENT	DESCRIPTION	MFR.	MFR. PART
H2510-01002-1/16W1-T	2	ea	R46, R1034		RES, SMD, 0402, 10k, 1/16W, 1%, TF, ROHS	PANASONIC	ERJ-2RKF1002X
H2510-02000-1/16W1-T	2	ea	R27, R1022	R1022 part of Vcm servo loop.	RES, SMD, 0402, 200Ω, 1/16W, 1%, TF, ROHS	PANASONIC	ERJ-2RKF2000X
H2510-02002-1/16W1-T	3	ea	R1032, R1033, R1042	R1032, R1033 part of Vcm servo loop	RES, SMD, 0402, 20k, 1/16W, 1%, TF, ROHS	PANASONIC	ERJ2RKF2001
H2510-02320-1/16W1-T	1	ea	R1021	ADC Vcm output pulldown	RES, SMD, 0402, 232Ω, 1/16W, 1%, TF, ROHS	VENKEL	CR0402-16W-2320FT
H2510-040R2-1/16W1-T	2	ea	R1013, R1014	Differential 3rd order filter first resistors	RES, SMD, 0402, 40.2Ω, 1/16W, 1%, TF, ROHS	PANASONIC	ERJ-2RKF40R2X
H2510-054R9-1/16W1-T	2	ea	R48, R49	Sync output series elements	RES, SMD, 0402, 54.9Ω, 1/16W, 1%, TF, ROHS	VISHAY/DALE	CRCW040254R9FKED
H2510-07151-1/16W1-T	1	ea	R1044		RES, SMD, 0402, 7.15k, 1/16W, 1%, TF, ROHS	PANASONIC	ERJ-2RKF7151X
H2510-095R3-1/10W1-T	2	ea	R50, R51	Sync output shunt elements	RES, SMD, 0402, 95.3Ω, 1/16W, 1%, TF, ROHS	PANASONIC	ERJ-2RKF95R3X
H2510-DNP	0	ea	a) R3, R35, R16, R14 R15, R40, R41, R1019		RES, SMD, 0402, DNP, DNP, DNP, TF, ROHS		
H2510-DNP	0	ea	b) Rbypass1-Rbypass4, Rterm1,	Optional bypass elements around input transformers	RES, SMD, 0402, DNP, DNP, DNP, TF, ROHS		
H2511-00R00-1/10W-T	3	ea	R32, R33, R1000		RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	VENKEL	CR0603-10W-000T
H2511-01001-1/10W1-T	2	ea	R62, R63		RES, SMD, 0603, 1k, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF1001V
H2511-01002-1/10W1-T	1	ea	R34		RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	KOA	RK73H1JT1002F
H2511-026R7-1/10W1-T	2	ea	R1016, R1017	Sense path divider output to 1:1 transformer	RES, SMD, 0603, 26.7Ω, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF26R7V
H2511-04701-1/10W1-T	6	ea	R2, R29, R31, R37, R39, R61		RES, SMD, 0603, 4.7k, 1/10W, 1%, TF, ROHS	YAGEO	9C06031A4701FKHFT
H2511-049R9-1/10W1-T	1	ea	Rterm3	Disable input (ISL55210) termination to ground at logic gate	RES, SMD, 0603, 49.9Ω, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-49R9FT
H2511-05490-1/10W1-T	2	ea	R1015, R1018	Sense path divider output to 1:1 transformer	RES, SMD, 0603, 549Ω, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-5490FT
H2511-DNP	0	ea	R1001, R1002, R1004, R1005, Rterm2	Alternate Vcm setup for fixed clock and divider to disable logic input	RES, SMD, 0603, DNP-PLACE HOLDER, ROHS		
RR0510P-4990-D-T	2	ea	R1008, R1011		RES, SMD, 0402, 499Ω, 1/16W, 0.5%, THINFILM, ROHS	SUSUMU CO., LTD	RR0510P-4990-D

ISLA214P50-55210EV1Z Bill of Materials ☐ Shaded rows unpopulated (Continued)

PART NUMBER	QTY	UNITS	REFERENCE DESIGNATOR	COMMENT	DESCRIPTION	MFR.	MFR. PART
B3FS-1000P-T	1	ea	SW1	ADC Reset button	SWITCH-PUSH, TH, 6MM, OFF-MOM, SPST-NO, 100GF, ROHS	OMRON	B3FS-1000P
ADT1-1WT+	1	ea	T4	Vtest path output transformer	TRANSFORMER-RF, SMD, 6P, CASE CD542, 0.5W, 30mA, ROHS	MINI-CIRCUITS	ADT1-1WT+
ADT4-6T+	1	ea	T1 *(PIN 1 AT UPPER LEFT CORNER)	Input step up transformer	TRANSFORMER, SMD, 6P, 7.8X5.5, 50Ω, 0.06-300MHz, ROHS	MINI-CIRCUITS	ADT4-6T+
ADTL1-12+	1	ea	T2 *(PIN 1 AT UPPER LEFT CORNER)	Input common mode choke transformer	TRANSFORM-RF, SMD, 6P, CASECD542, 20-1200MHz, 2W, ROHS	MINI-CIRCUITS	ADTL1-12+
TC4-19G2+-T	1	ea	T3	Transformer for clock input	TRANSFORMER-RF, SMD, 6P, AT224-3, 50Ω, 1/4W, 30mA, ROHS	MINI-CIRCUITS	TC4-19G2+
5X8-STATIC-BAG	1	ea	Place assy in bag.		BAG, STATIC, 5X8, ZIPLOC, ROHS	INTERSIL	212403-013
DNP	0	ea	J5, J7	SMA	DO NOT POPULATE OR PURCHASE		
DNP	0	ea	L1004	Optional filter for BP design to ADC	DO NOT POPULATE OR PURCHASE		
DNP	0	ea	Pd Vtest	SMA	DO NOT POPULATE OR PURCHASE		
DNP	0	ea	R1003	2kΩ 10 turn pot for the ISL55210 Vcm control path.	DO NOT POPULATE OR PURCHASE		
DNP	0	ea	R22-R26, R28		DO NOT POPULATE OR PURCHASE		
DNP	0	ea	U6, U8, U9	ADCLK905 for U8, U9	DO NOT POPULATE OR PURCHASE		
LABEL-SERIAL NUMBER	1	ea	AFFIX LABEL TO BOTTOM OF PCB		LABEL-FOR SERIAL NUMBER AND BOM REV #	INTERSIL	LABEL-SERIAL NUMBER