

Protection Devices

TVS (Transient Voltage Suppressor Diodes)

ESD108-B1-CSP0201

Bi-directional, 5.5 V, 0.28 pF, 0201, RoHS and Halogen Free compliant

ESD108-B1-CSP0201

Data Sheet

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1 Product Overview

1.1 Features

- ESD / transient protection of high speed data lines according to:
 - IEC61000-4-2 (ESD): ± 25 kV (air/contact discharge)
 - IEC61000-4-4 (EFT): ± 2.5 kV / ± 50 A (5/50 ns)
 - IEC61000-4-5 (surge): ± 2.5 A (8/20 μ s)
- Bi-directional working voltage up to: $V_{RWM} = \pm 5.5$ V
- Line capacitance: $C_L = 0.28$ pF (typical) at $f = 1$ MHz
- Clamping voltage: $V_{CL} = 20$ V (typical) at $I_{TLP} = 16$ A with $R_{DYN} = 0.78 \Omega$ (typical)
- Very low reverse current: $I_R < 1$ nA (typical)
- Minimized clamping overshoot due to extremely low parasitic inductance
- Small form factor SMD Size 0201 and low profile (0.58 mm x 0.28 mm x 0.15 mm)
- Bidirectional and symmetric I/V characteristics for optimized design and assembly
- Pb-free (RoHS compliant) and halogen free package



Guidelines for optimized PCB design and assembly process available [\[2\]](#)



1.2 Application Examples

- USB 3.0, Firewire, DVI, HDMI, S-ATA, DisplayPort, Thunderbolt
- Mobile HDMI Link, MDDI, MIPI, SWP / NFC
- Dedicated solution to boost space saving and high performance in miniaturized modern electronics

1.3 Product Description

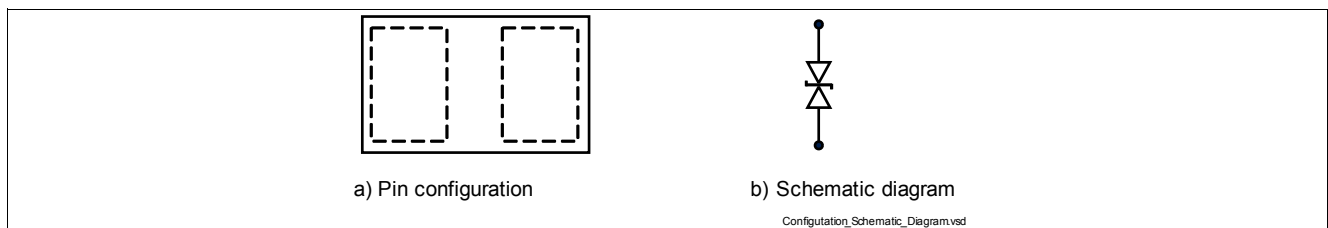


Figure 1-1 Pin Configuration and Schematic Diagram

Table 1-1 Part Information

Type	Package	Configuration	Marking code
ESD108-B1-CSP0201	WLL-2-1	1 line, bi-directional	C ¹⁾

1) The device does not have any marking or date code on the device backside. The Marking code is on pad side.

2 Maximum Ratings

Table 2-1 Maximum Ratings at $T_A = 25\text{ °C}$, unless otherwise specified ¹⁾

Parameter	Symbol	Values	Unit
Reverse working voltage	V_{RWM}	±5.5	
ESD (air / contact) discharge ²⁾	V_{ESD}	±25	kV
Reverse working current	I_{RWM}	10	mA
Peak pulse power $t_p = 8 / 20\ \mu\text{s}$ ³⁾ $t_p = 100\ \text{ns}$ ²⁾	P_{PK}	27.5 18000	W
Peak pulse current ³⁾	I_{PP}	±2.5	A
Operating temperature range	T_{OP}	-55 to 125	°C
Storage temperature	T_{stg}	-65 to 150	°C

1) Device is electrically symmetrical

2) V_{ESD} according to IEC61000-4-2 ($R = 330\ \Omega$, $C = 150\ \text{pF}$ discharge network)

3) Stress pulse: 8/20 μs current waveform according to IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component.

Table 2-2 Thermal Resistance

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Junction - soldering point ¹⁾	R_{thJS}	-	-	330	K/W

1) For calculation of R_{thJA} please refer to Application Note [\[3\]](#) 077 Thermal Resistance Calculation.

Electrical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

3 Electrical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

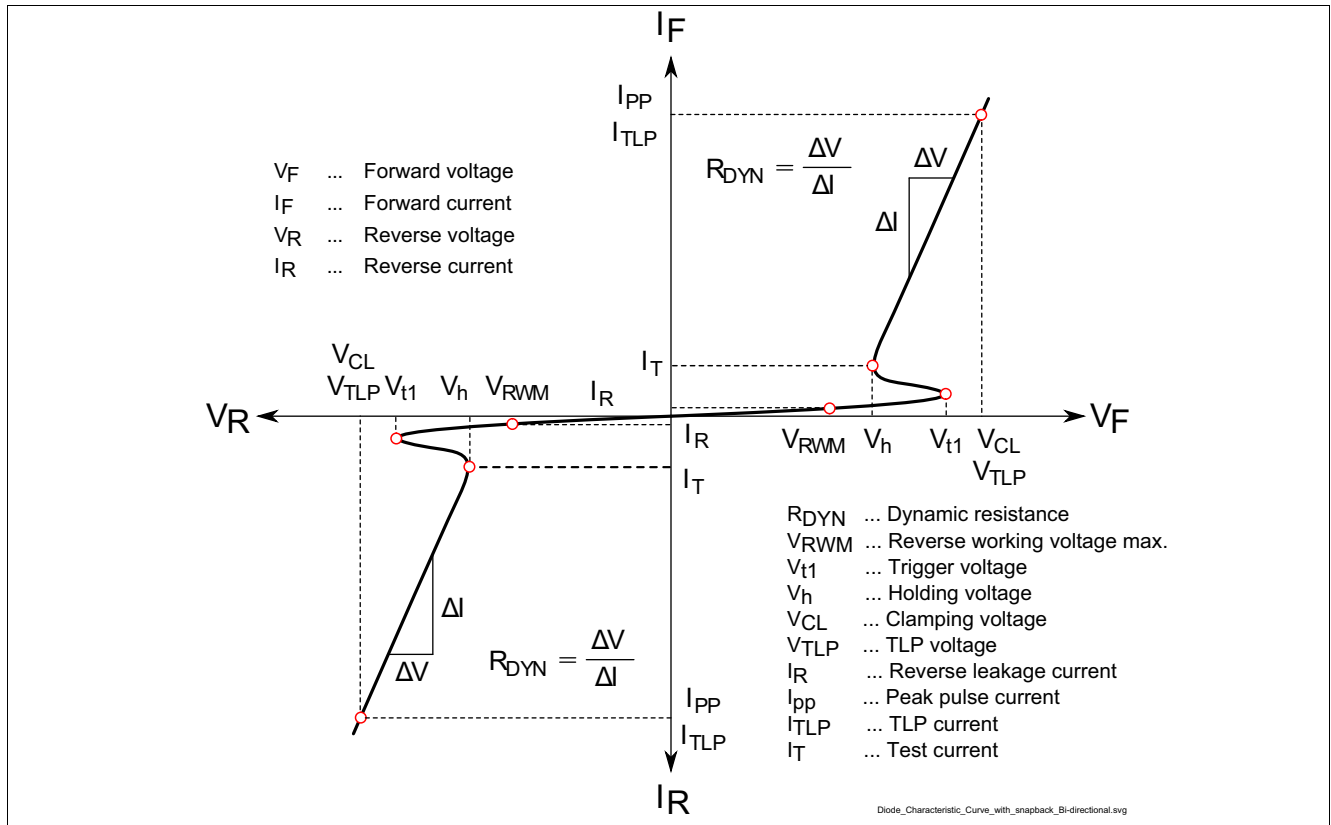


Figure 3-1 Definitions of electrical characteristics

Table 3-1 DC Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse current	I_R	–	<1	20	nA	$V_R = \pm 5.5\text{ V}$
Trigger voltage	V_{t1}	–	9.5	12.5	V	
Holding voltage	V_h	5.5	6.5	9.5	V	$I_T = 0.5\text{ mA}$

1) Device is electrically symmetrical

Table 3-2 AC Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	0.28	0.38	pF	$V_R = 0\text{ V}, f = 1\text{ MHz}$
		–	0.22	0.38		$V_R = 0\text{ V}, f = 1\text{ GHz}$

Electrical Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified
Table 3-3 ESD and Surge Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified ¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage ²⁾	V_{CL}	–	20	27	V	$I_{TLP} = 16\text{ A}$, $t_p = 100\text{ ns}$
		–	30.5	41		$I_{TLP} = 30\text{ A}$, $t_p = 100\text{ ns}$
Clamping voltage ³⁾		–	20	–		$V_{ESD} = 8\text{ kV}$
		–	29	–		$V_{ESD} = 15\text{ kV}$
Clamping voltage ⁴⁾		–	8.5	12		$I_{PP} = 1\text{ A}$, $t_p = 8/20\text{ }\mu\text{s}$
		–	11	18.5		$I_{PP} = 2.5\text{ A}$, $t_p = 8/20\text{ }\mu\text{s}$
Dynamic resistance ²⁾	R_{DYN}	–	0.78	–	Ω	$t_p = 100\text{ ns}$

1) Device is electrically symmetrical

2) Please refer to Application Note AN210[1]. TLP parameter: $Z_0 = 50\text{ }\Omega$, $t_p = 100\text{ ns}$, $t_r = 0.6\text{ ns}$

3) V_{ESD} according to IEC61000-4-2 (contact discharge), V_{CL} at 30 ns ($R = 330\text{ }\Omega$, $C = 150\text{ pF}$ discharge network)

4) Stress pulse: 8/20 μs current waveform according to IEC61000-4-5

4 Typical Characteristics Diagrams

Typical characteristics diagrams at $T_A = 25\text{ °C}$, unless otherwise specified

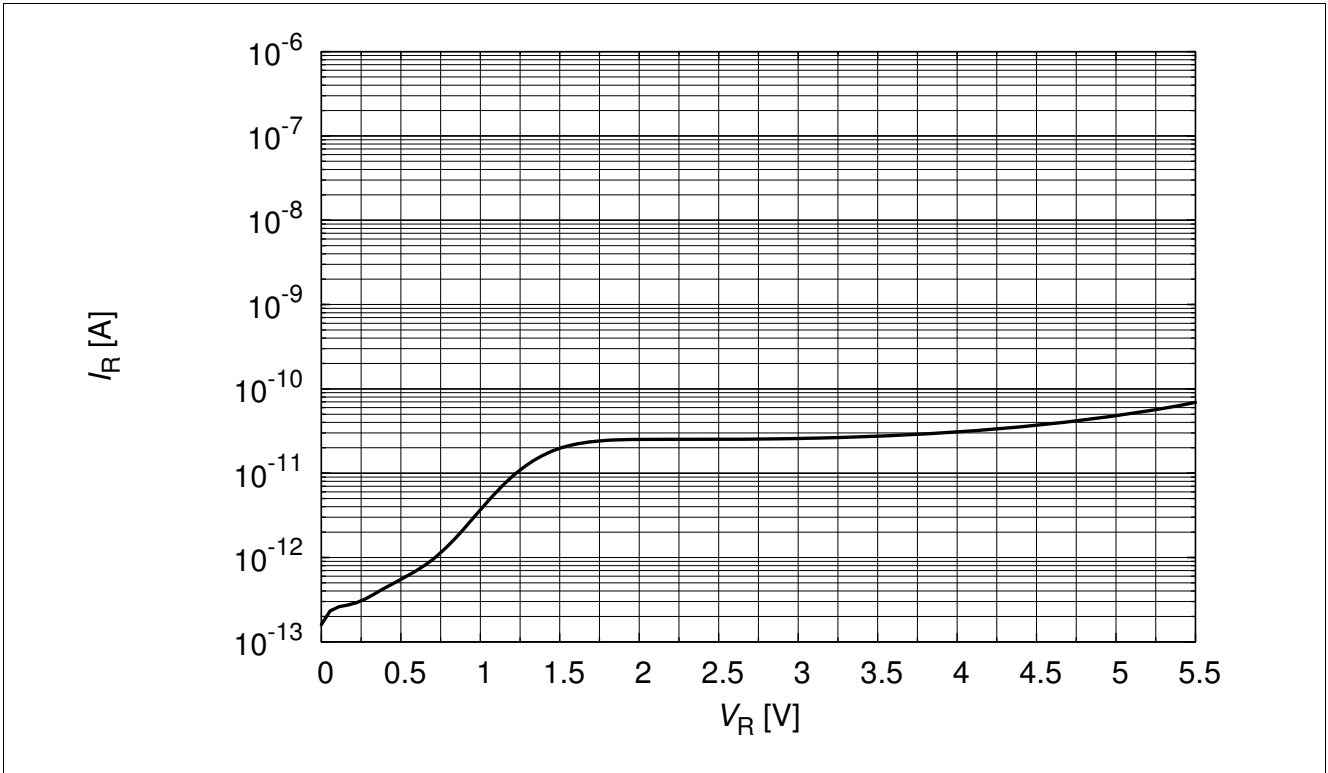


Figure 4-1 Reverse leakage current $I_R = f(V_R)$

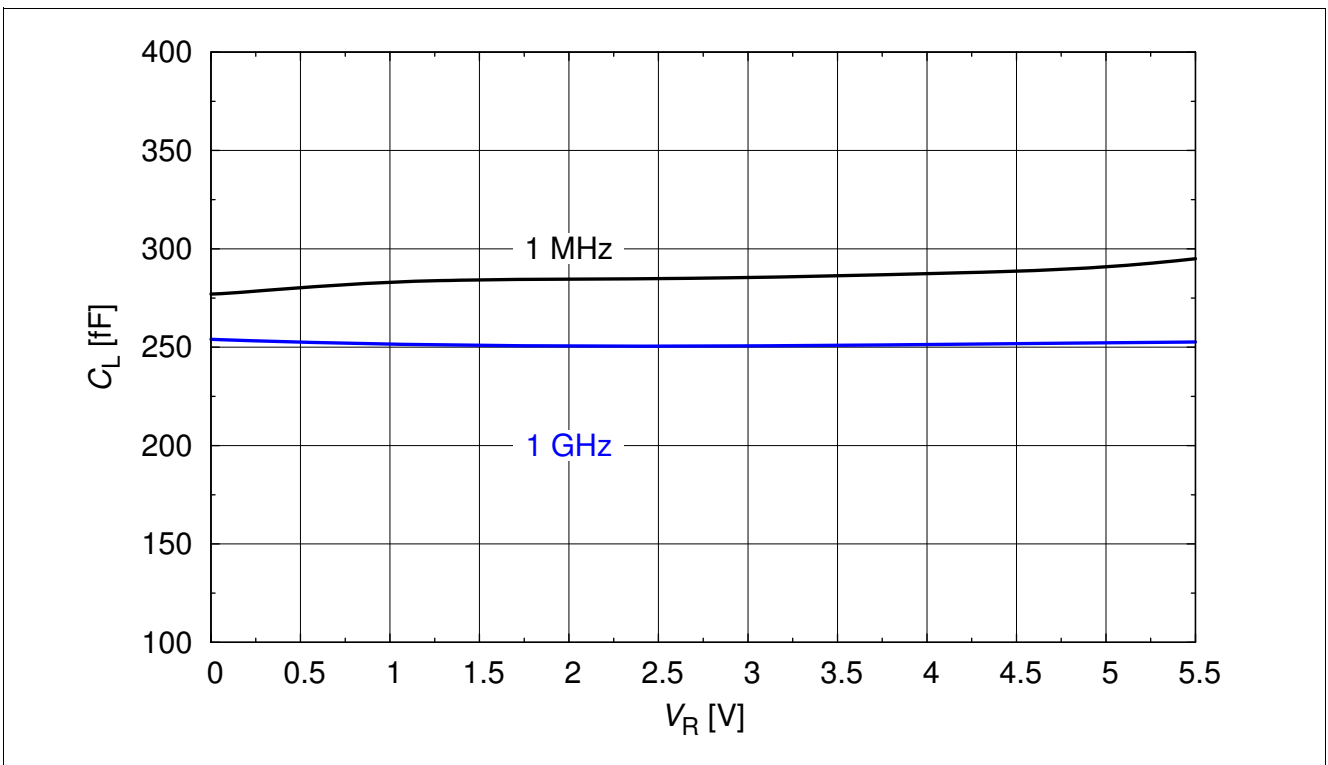


Figure 4-2 Line capacitance $C_L = f(V_R)$

Typical Characteristics Diagrams

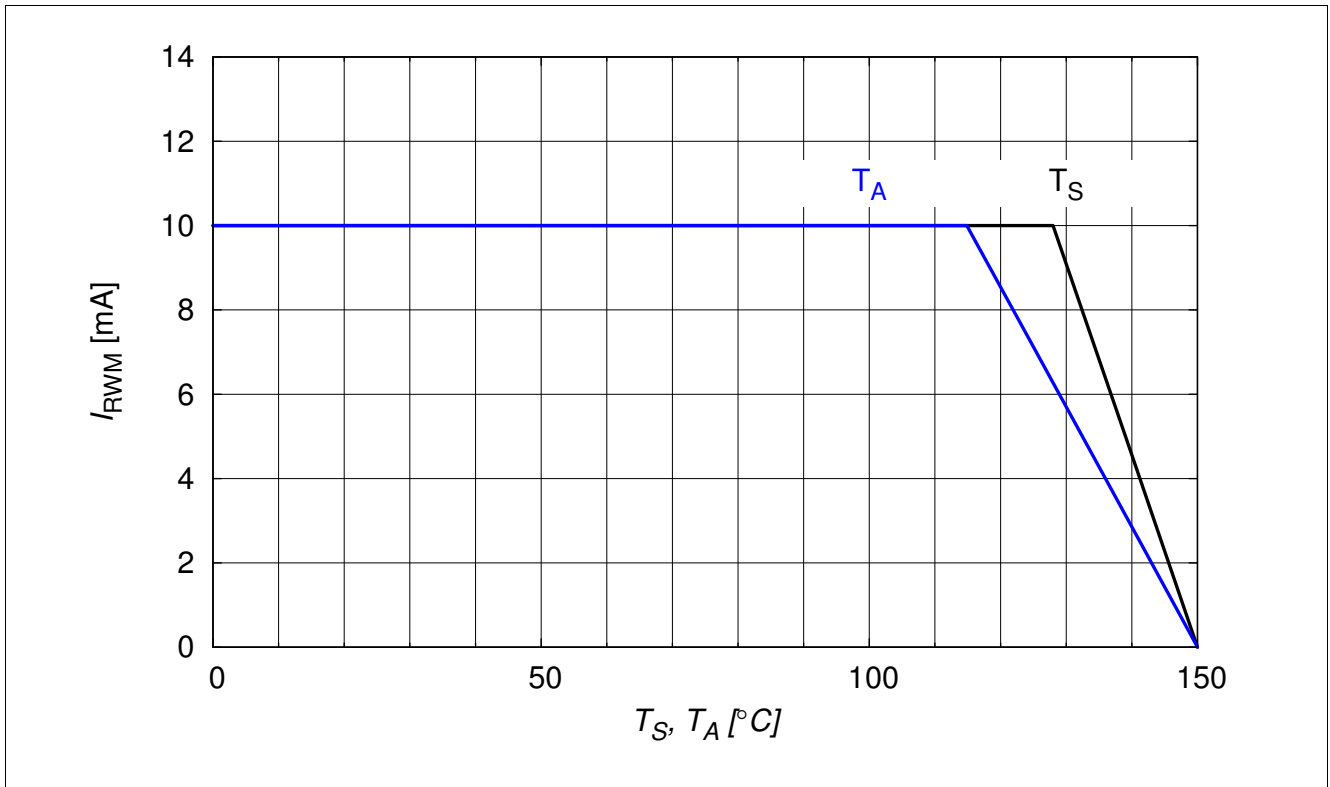


Figure 4-3 Reverse working current $I_{RWM} = f(T_S, T_A)$, Device mounted on PCB with $R_{th} = 200$ K/W [3]

Typical Characteristics Diagrams

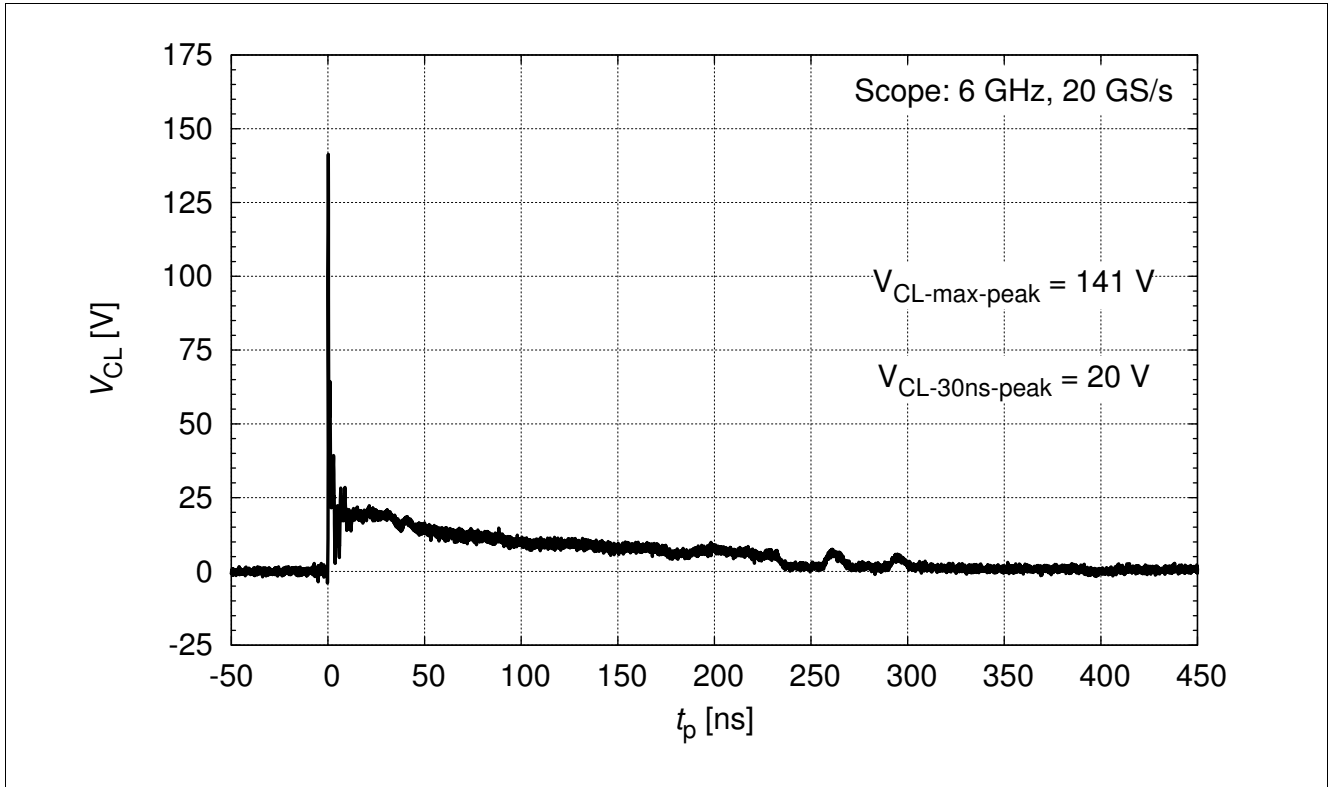


Figure 4-4 Clamping voltage (ESD): $V_{CL} = f(t)$, 8 kV positiv pulse

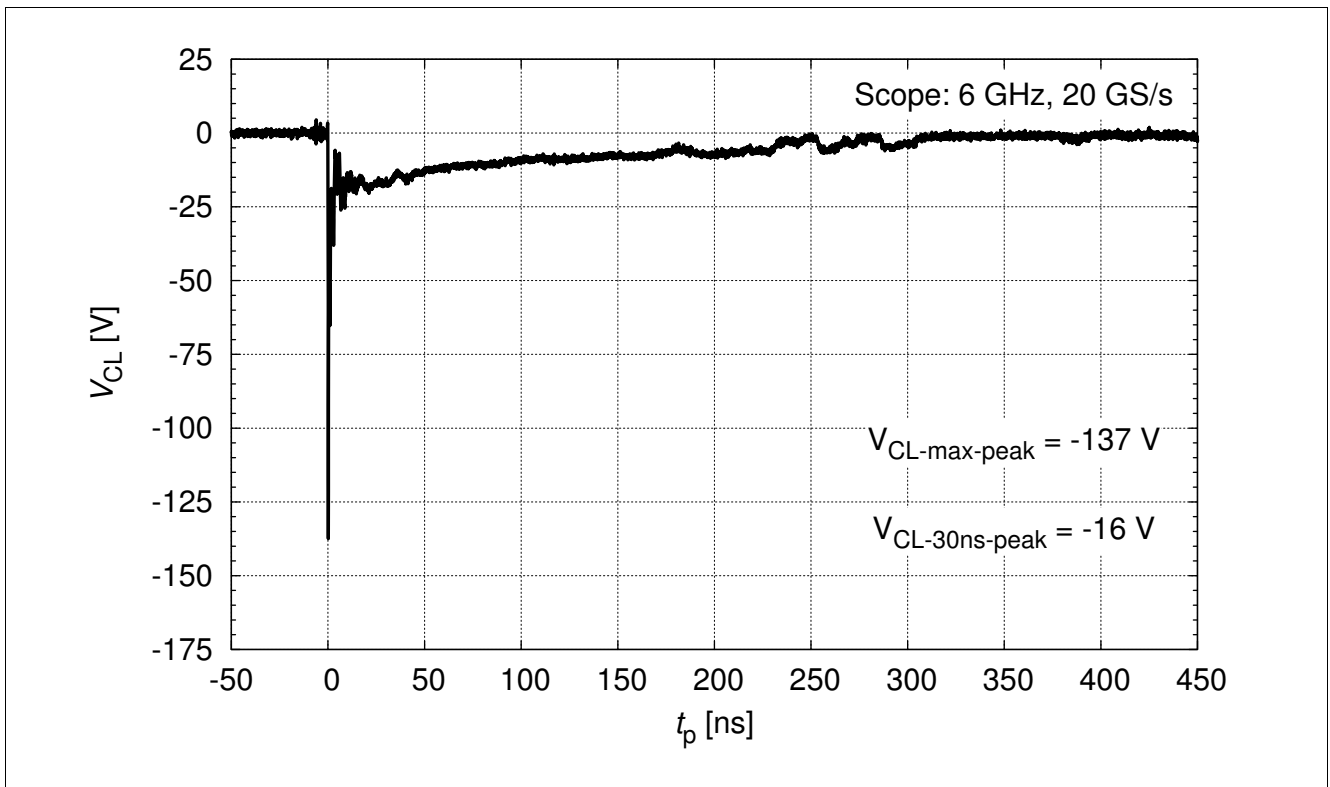


Figure 4-5 Clamping voltage (ESD): $V_{CL} = f(t)$, 8 kV negativ pulse

Typical Characteristics Diagrams

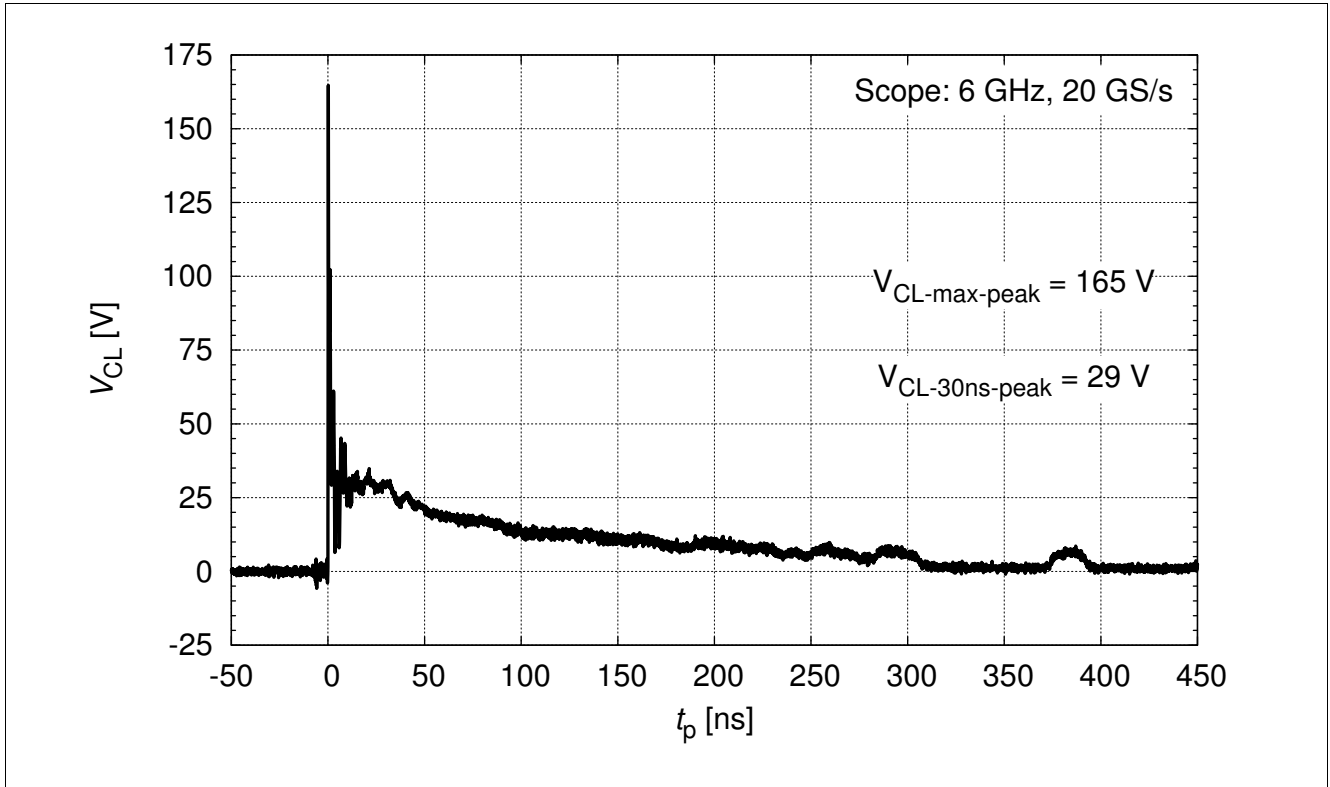


Figure 4-6 Clamping voltage (ESD): $V_{CL} = f(t)$, 15 kV positiv pulse

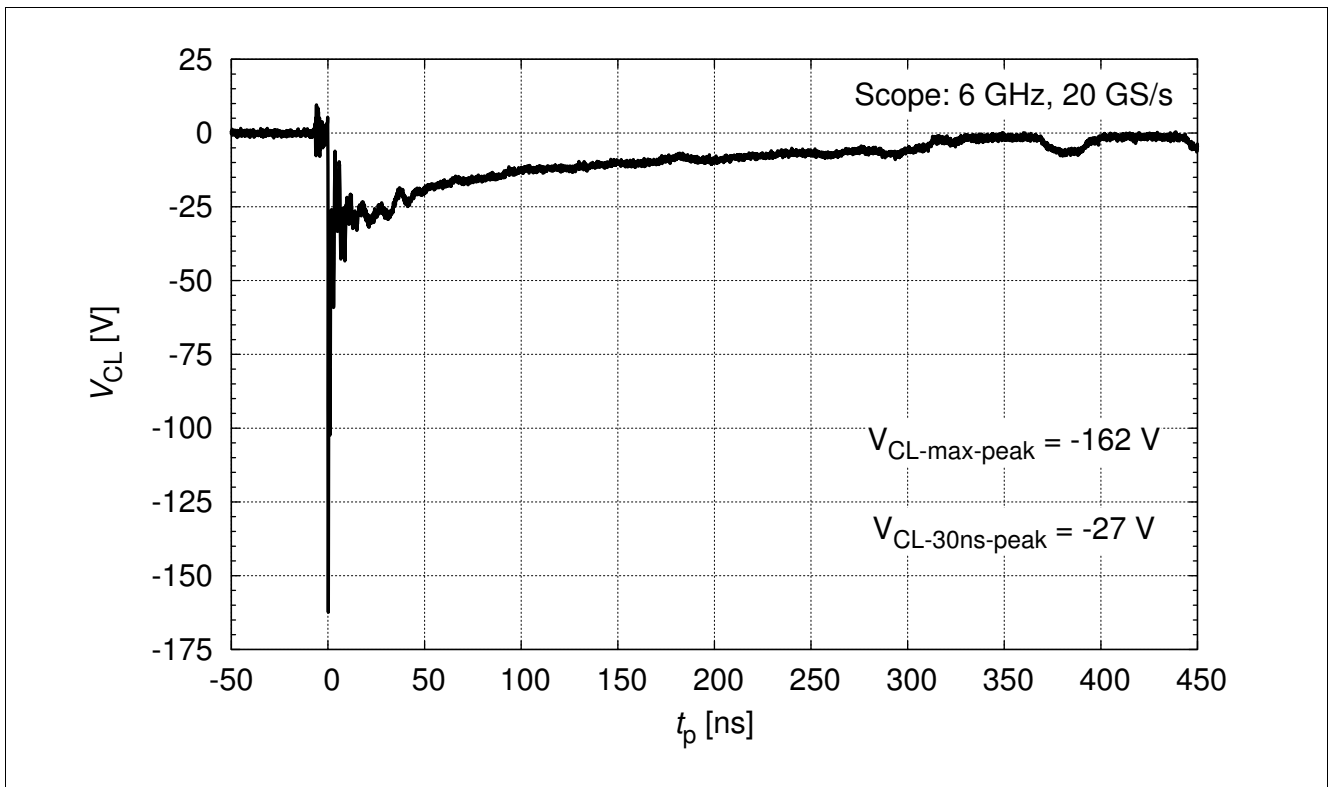


Figure 4-7 Clamping voltage (ESD): $V_{CL} = f(t)$, 15 kV negativ pulse

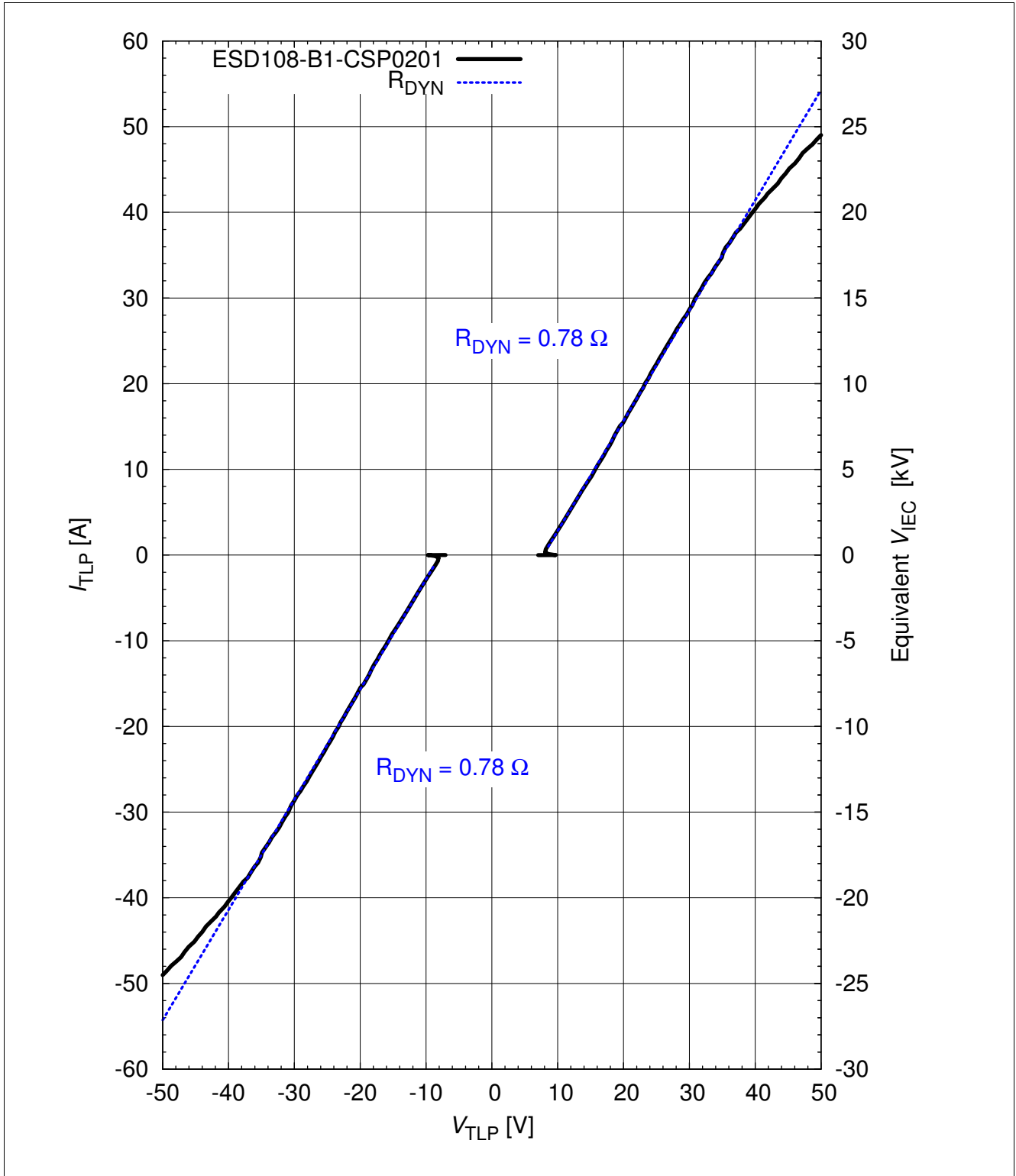


Figure 4-8 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ [1]

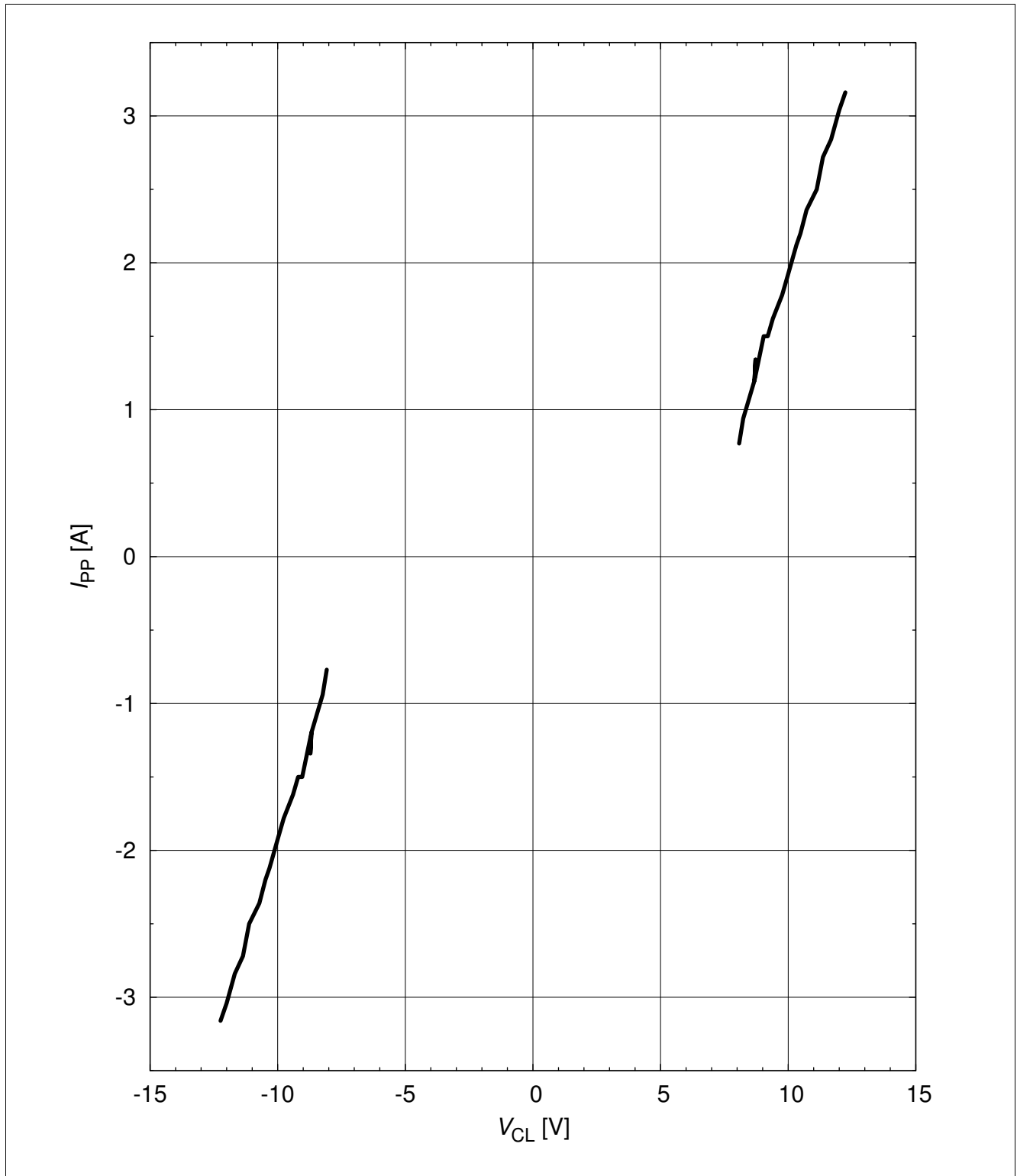


Figure 4-9 Clamping voltage (Surge): $I_{PP} = f(V_{CL})$ [1]

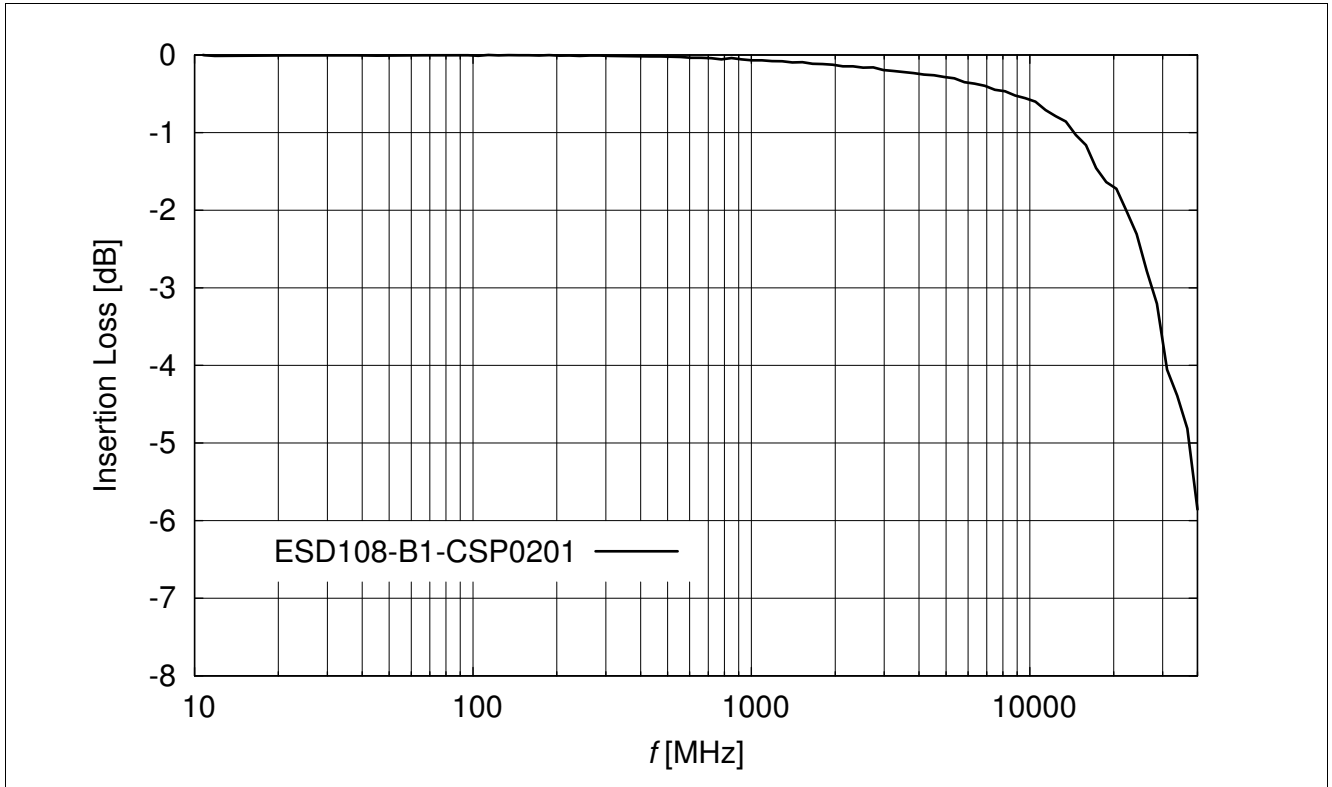


Figure 4-10 Insertion loss vs. frequency in a 50 Ω system

5 Package Information

5.1 WLL-2-1

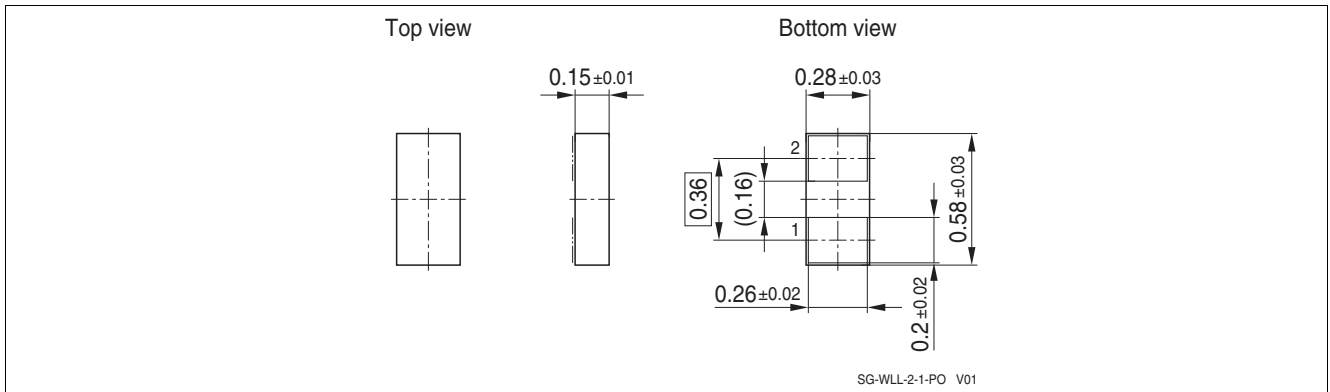


Figure 5-1 WLL-2-1 Package outline (dimension in mm)

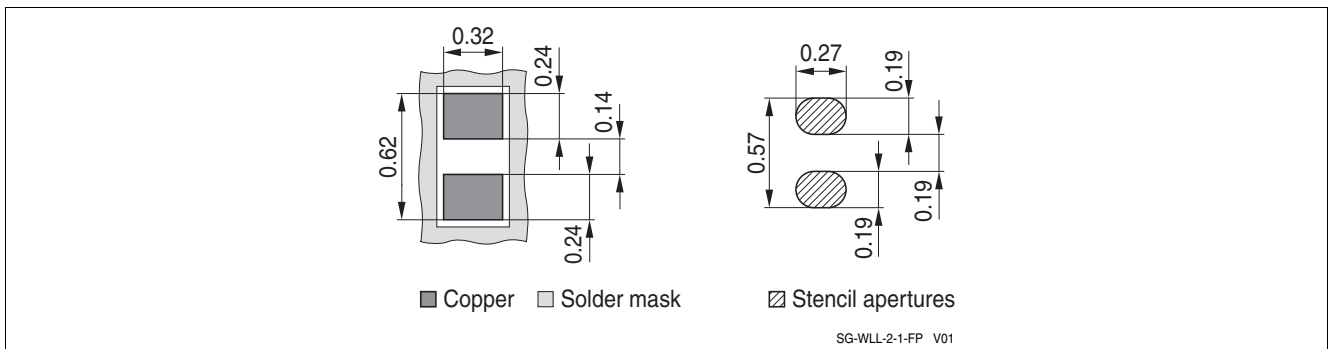


Figure 5-2 WLL-2-1 Footprint (dimension in mm) Recommendation for Printed Circuit Board Assembly[2]

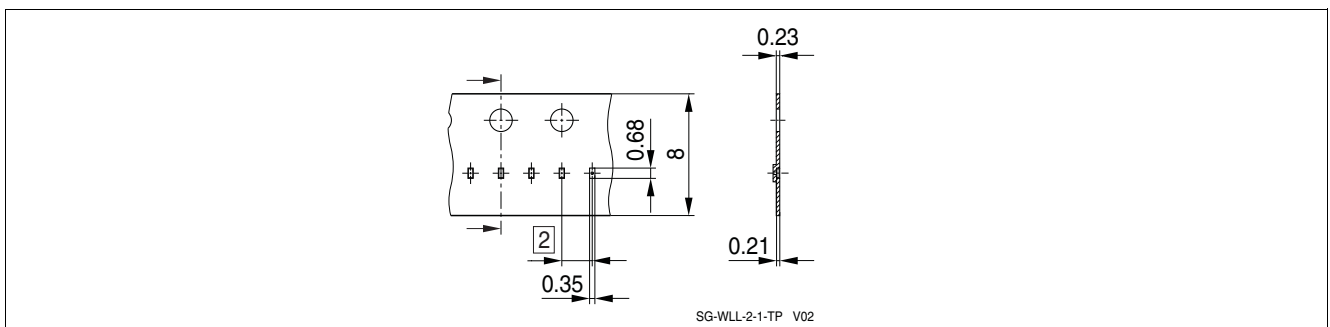


Figure 5-3 WLL-2-1 Packing (dimension in mm)

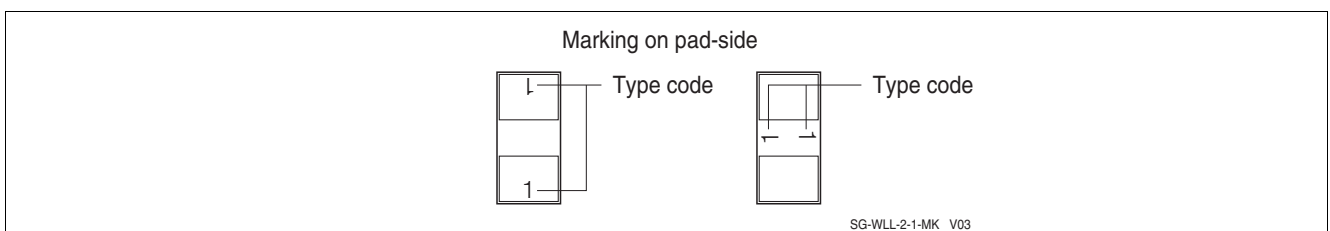


Figure 5-4 WLL-2-1 Marking example Table 1-1 "Part Information" on Page 3

References

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology
- [2] Infineon AG - Recommendation for Printed Circuit Board Assembly of Infineon WLL Packages
<http://www.infineon.com/dgdl/?fileId=db3a304344f7b4f9014503db540027c0>
- [3] Infineon AG - **Application Note AN077**: Thermal Resistance Calculation
- [4] Infineon AG - **Application Note AN392**: TVS Diodes in ChipScalePackage reduce size and save cost

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Page or Item	Subjects (major changes since previous revision)
Revision 1.4, 2016-04-21	
All	Layout update

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