TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (Ultra-High-Speed U-MOS III)

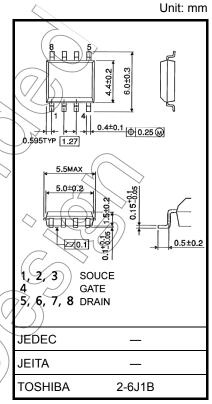
# **TPC8022-H**

High-Efficiency DC/DC Converter Applications Notebook PC Applications Portable-Equipment Applications CCFL Inverter Applications

- Small footprint due to a small and thin package
- High speed switching
- Small gate charge: QSW = 3.5 nC (typ.)
- Low drain-source ON-resistance: RDS (ON) =  $22 \text{ m}\Omega$  (typ.)
- High forward transfer admittance:  $|Y_{fs}| = 15 S$  (typ.)
- Low leakage current:  $IDSS = 10 \mu A (max) (VDS = 40 V)$
- Enhancement mode:  $V_{th} = 1.1 \text{ to } 2.3 \text{ V } (V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA})$

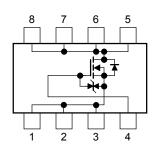
## Absolute Maximum Ratings (Ta = 25°C)

Characteristic			Symbol	Rating	Unit
Drain-source voltage			V <sub>DSS</sub> <	40	/y
Drain-gate voltage ( $R_{GS}$ = 20 k $\Omega$ )			V <sub>DGR</sub>	40	<\u20e4\u20e4
Gate-source voltage			V <sub>GSS</sub>	±20	V
Drain current	DC	(Note 1)	₽ A	7.5	\ A
	Pulse	(Note 1)	((IDP))	30	
Drain power dissipation (t = 10 s) (Note 2a)			PD	1.9	W
Drain power dissipation (Note 2b)			PD	(1.0)	W
Single-pulse avalanche energy (Note 3)			EAS	26	mJ
Avalanche current			I <sub>AR</sub>	7.5	Α
Repetitive avalanche energy Single-device value at dual operation (Note 2a, 4)			EAR	0.08	mJ
Channel temperature			T <sub>ch</sub>	150	°C
Storage temperature range			T <sub>stg</sub>	-55 to 150	°C



Weight: 0.085 g (typ.)

### **Circuit Configuration**



Note: For Notes 1 to 4, refer to the next page.

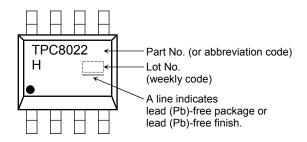
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Handle with care.

#### **Thermal Characteristics**

Characteristic	Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 10 s) (Note 2a)	R <sub>th (ch-a)</sub>	65.8	°C/W
Thermal resistance, channel to ambient (t = 10 s) (Note 2b)	R <sub>th (ch-a)</sub>	125	C/VV

### Marking (Note 5)

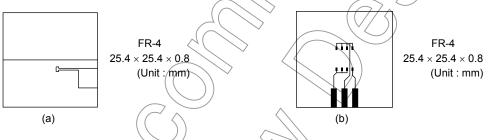


Note 1: The channel temperature should not exceed 150°C during use

Note 2:

a) Device mounted on a glass-epoxy board (a)

Device mounted on a glass-epoxy board (b)



Note 3:  $V_{DD} = 24 \text{ V}$ ,  $T_{ch} = 25^{\circ}\text{C}$  (initial), L = 0.5 mH,  $R_G = 25 \Omega$ ,  $I_{AR} = 7.5 \text{ A}$ 

Note 4: Repetitive rating: pulse width limited by maximum channel temperature

Note 5: • on the lower left of the marking indicates Pin 1.

\* Weekly code: (Three digits)

Week of manufacture

(01 for first week of year, continuing up to 52 or 53)

2

Year of manufacture

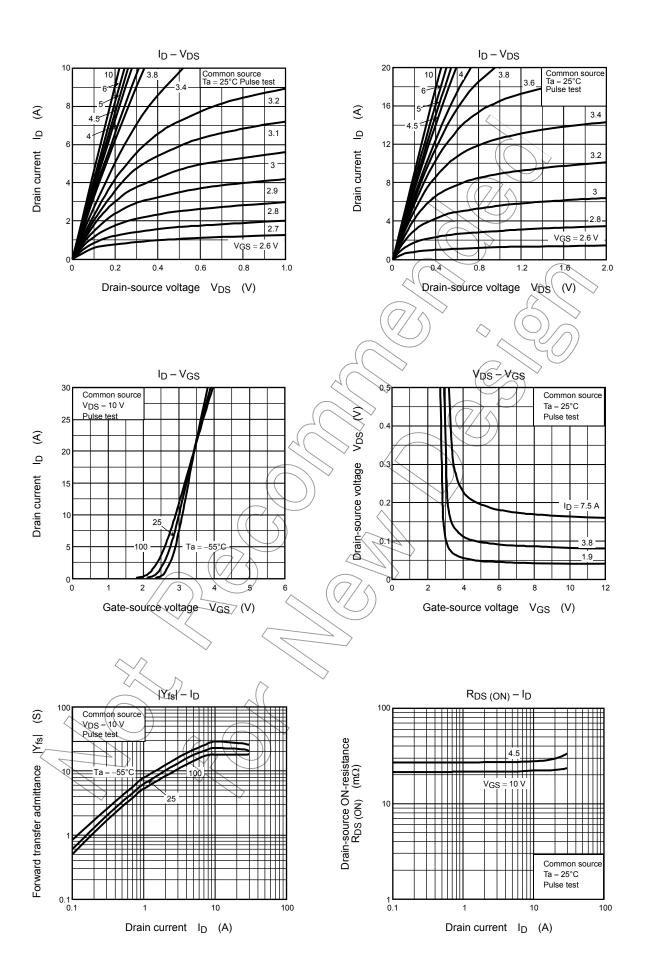
(The last digit of the calendar year)

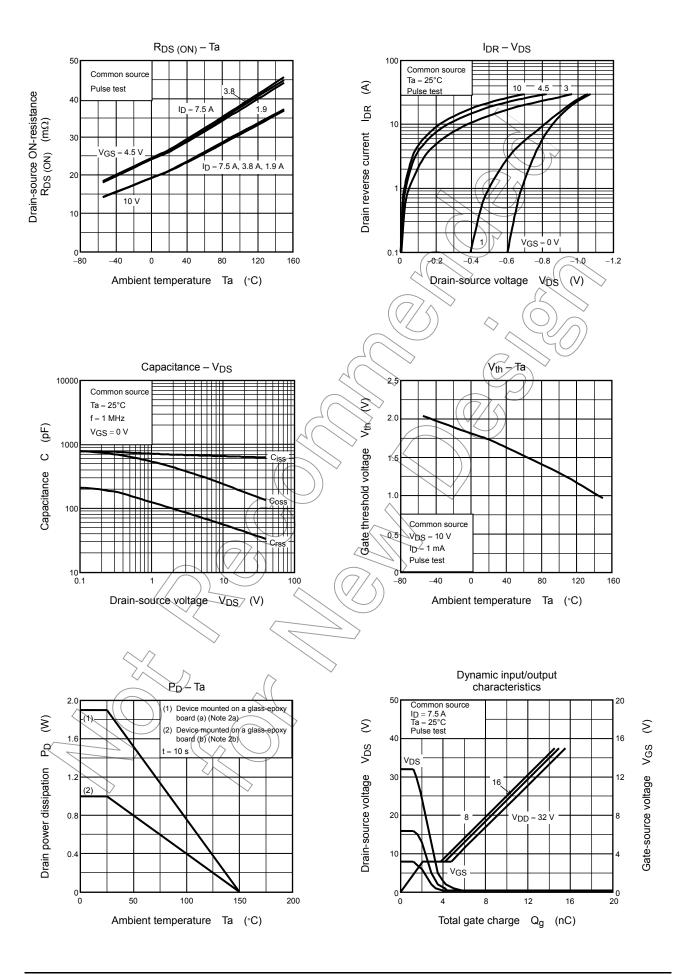
### Electrical Characteristics (Ta = 25°C)

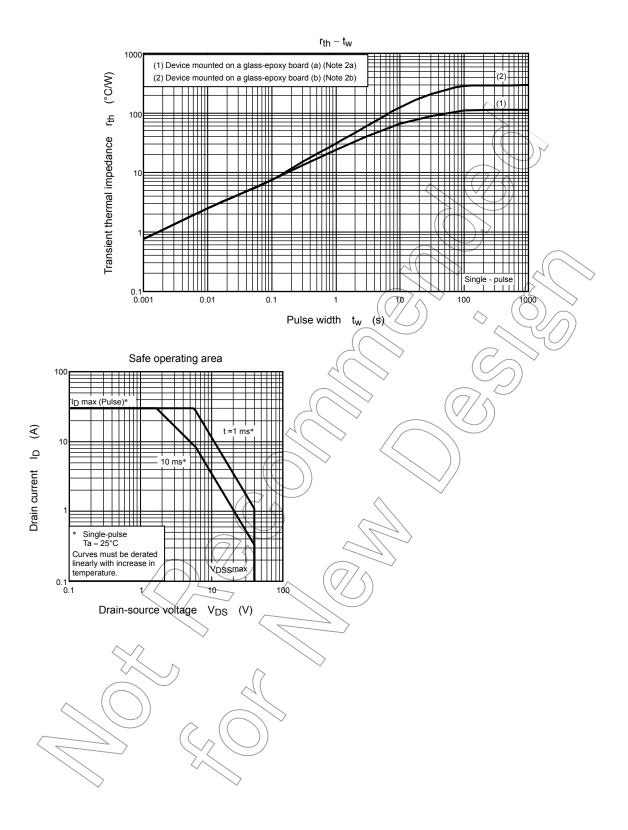
Characteristic		Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current		I <sub>GSS</sub>	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0 V	_	_	±10	μΑ
Drain cutoff curr	ent	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V	_	_	10	μΑ
Drain-source breakdown voltage		V (BR) DSS	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0 V	40	_	_	V
		V <sub>(BR) DSX</sub>	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = -20 V	25	1	_	v
Gate threshold	voltage	$V_{th}$	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	(1)	) >_	2.3	V
Drain-source ON-resistance		R <sub>DS (ON)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 3.8 A	) / />	27	35	mΩ
		R <sub>DS</sub> (ON)	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.8 A	$\rightarrow$	22	27	11177
Forward transfer admittance		Y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3.8 A	7.5	15	_	S
Input capacitano	ce	C <sub>iss</sub>		_	650	_	
Reverse transfe	r capacitance	C <sub>rss</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	_	55	_	pF
Output capacita	nce	Coss		- /	240	$\nearrow$	
Switching time	Rise time	tr	10 V D = 3.8 A		3	> _	
	Turn-on time	t <sub>on</sub>	V <sub>GS</sub> 10 V		>	_	
	Fall time	t <sub>f</sub>	V <sub>DD</sub> ≈ 20 V		2	_	ns
	Turn-off time	t <sub>off</sub>	Duty ≦ 1%, t <sub>w</sub> = 10 μs	-	18	_	
Total gate charge (gate-source plus gate-drain)		0 (	$V_{DD} \approx 32 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 7.5 \text{ A}$	-	11	_	
		Q <sub>g</sub> (	$V_{DD} \approx 32 \text{ V}, V_{GS} = 5 \text{ V}, I_D = 7.5 \text{ A}$	_	6.2	_	
Gate-source charge		Q <sub>gs1</sub>		_	2.1	_	nC
Gate-drain ("Miller") charge		Qgd	$V_{DD} \approx 32 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 7.5 \text{ A}$	_	2.7	_	
Gate switching charge		Qsw		_	3.5	_	

# Source-Drain Ratings and Characteristics (Ta = 25°C)

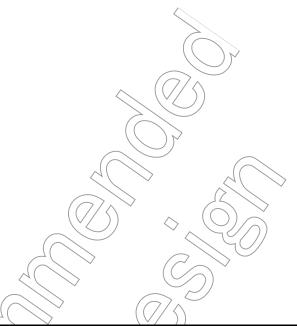
Characteristic Symbol Test Condition	Min	Тур.	Max	Unit
Drain reverse current Pulse (Note 1) I <sub>DRP</sub> —	ı	ı	30	Α
Forward voltage (diode) V <sub>DSF</sub> (I <sub>DR</sub> = 7.5 A, V <sub>GS</sub> = 0 V	_	_	-1.2	V







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